

TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG,CPU-Memory	3,4
CPU-Power,CPU-GND	5,6
SO_DDRIII DIMMA1&SO_DDRIII DIMMB1	7,8
PPT-PCI/E/DMI/CLK/USB20/USB30	9
PPT-SATA/HOST/GPIO/VGA/CCMOS	10
PPT-SMB/LPC/AUDIO/RTC/SPI	11
PPT-POWER,GND/NVRAM /CP STRAPS	12,13,14
PCIE Slot	15
PCI Slot	16
LAN - RTL8111E/8105	17
AUDIO 887	18
VGA/HDMI	19,20
USB2.0/3.0 Connector/SATA Connector	21,22,23
SIO-Fintek F71868AD	24
FAN	25
ATX F_Panel/EMI/TPM	26
ACPI Controller UPI	27
VRM12 - UT501colay UT1654P	28
UP6282 3-Phase+MOS CPU	29
UP6282 1-Phase+MOS GPU	30
UP1513 - VTT POWER	31
OP+MOS - SA POWER	32
UP1513 - DDR POWER	33
PCH POWER	34
ME Power - UP1712	35
XDP / Manual Parts	36
EMI CAP	37

MS-7808

ATX

Ver:0A

H/W:Frankyang

PM:Feifei

Intel -MahoBay plamform B75

CPU:

System Chipset:

IVY bridge LGA1155

Panther Point B75

Onboard Chip:

Audio Codec: 887

LAN-RTL8111E colay8105E

SIO:Fintek F71868AD

Flash ROM: SPI 128 MB

Main Memory:

DDRIII (1066/1333/1600MHz) * 2 (Dual Channel)

ACPI:

PWM:

UPI

VRD12 -UT501 3+1 Phase

Expansion Slots:

Other:

PCI Express (X16) Slot * 1

SATA3.0 x1+SATA2.0 x3 (PCH)

PCI Express (X1) Slot * 1

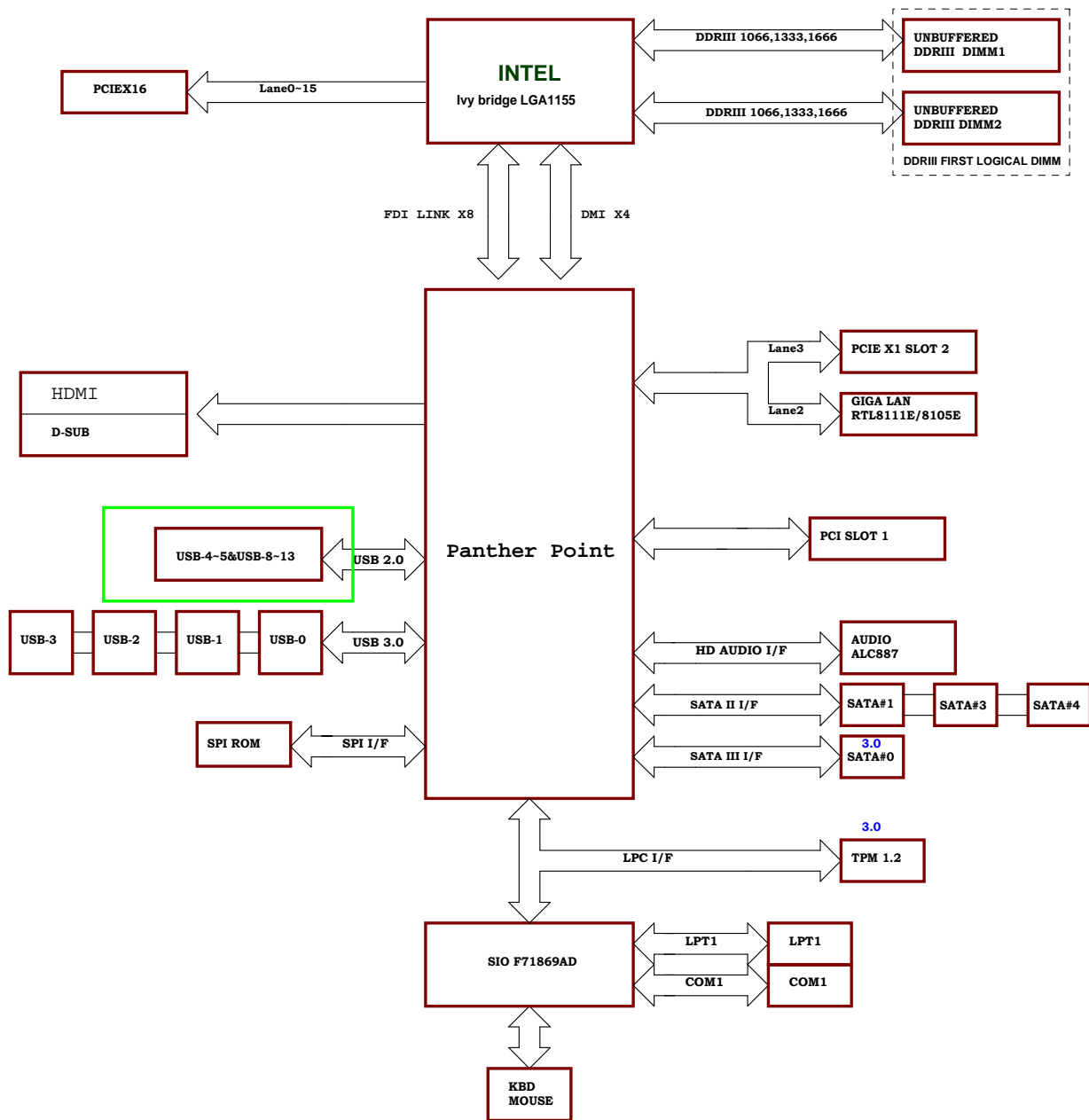
USB2.0 *8

PCI Slot * 1

REAL USB3.0 *2

FRONT USB3.0 *2

MS-7758 Block Diagram



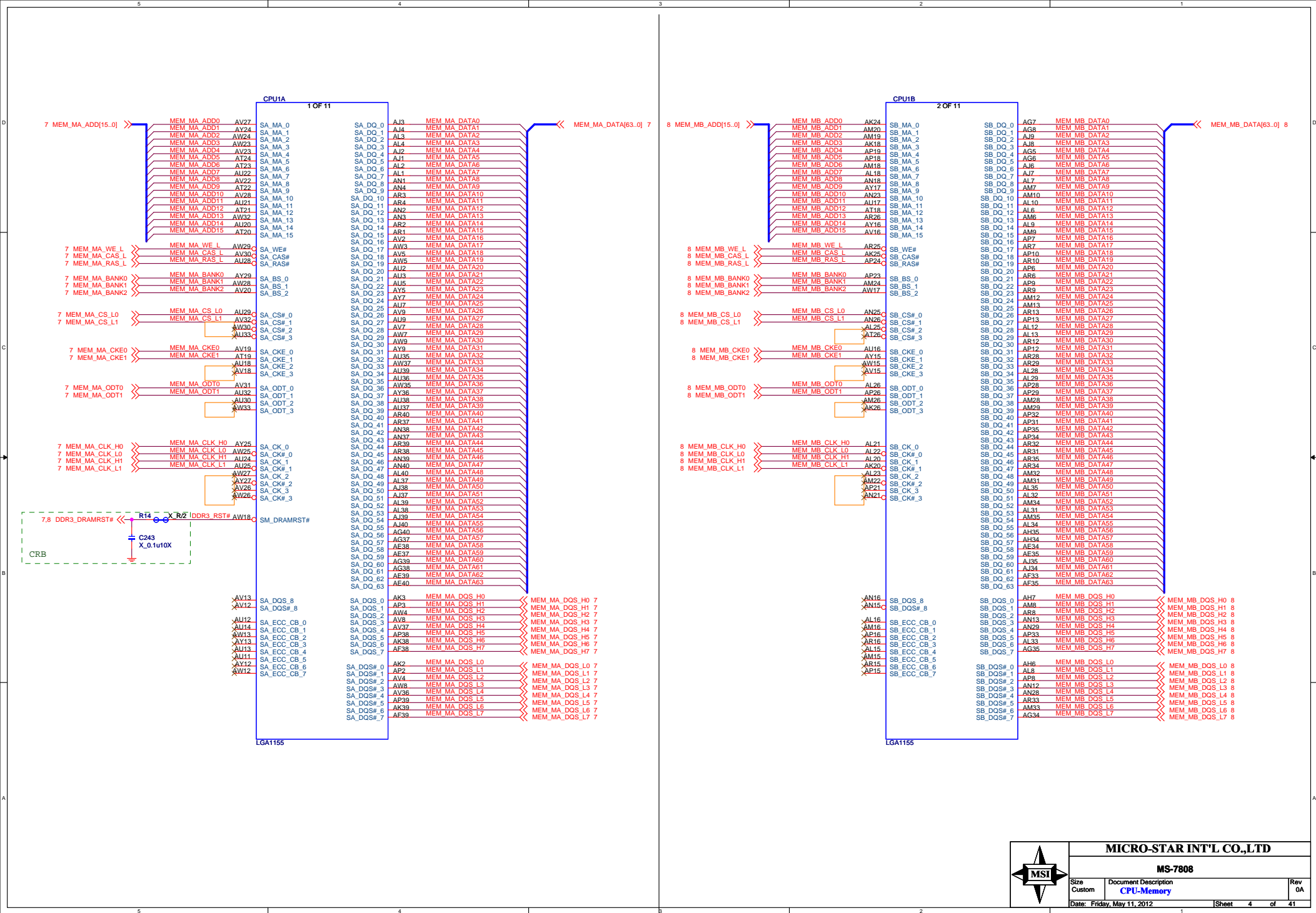
Slot Sequence:

- PCIEX16
- PCIEX1
- PCI SLOT



MICRO-STAR INT'L CO.,LTD		
MS-7808		
Size Custom	Document Description Block Diagram	Rev 0A
Date: Friday, May 11, 2012		Sheet 2 of 41





MICRO-STAR INT'L CO.,LTD

MS-7808

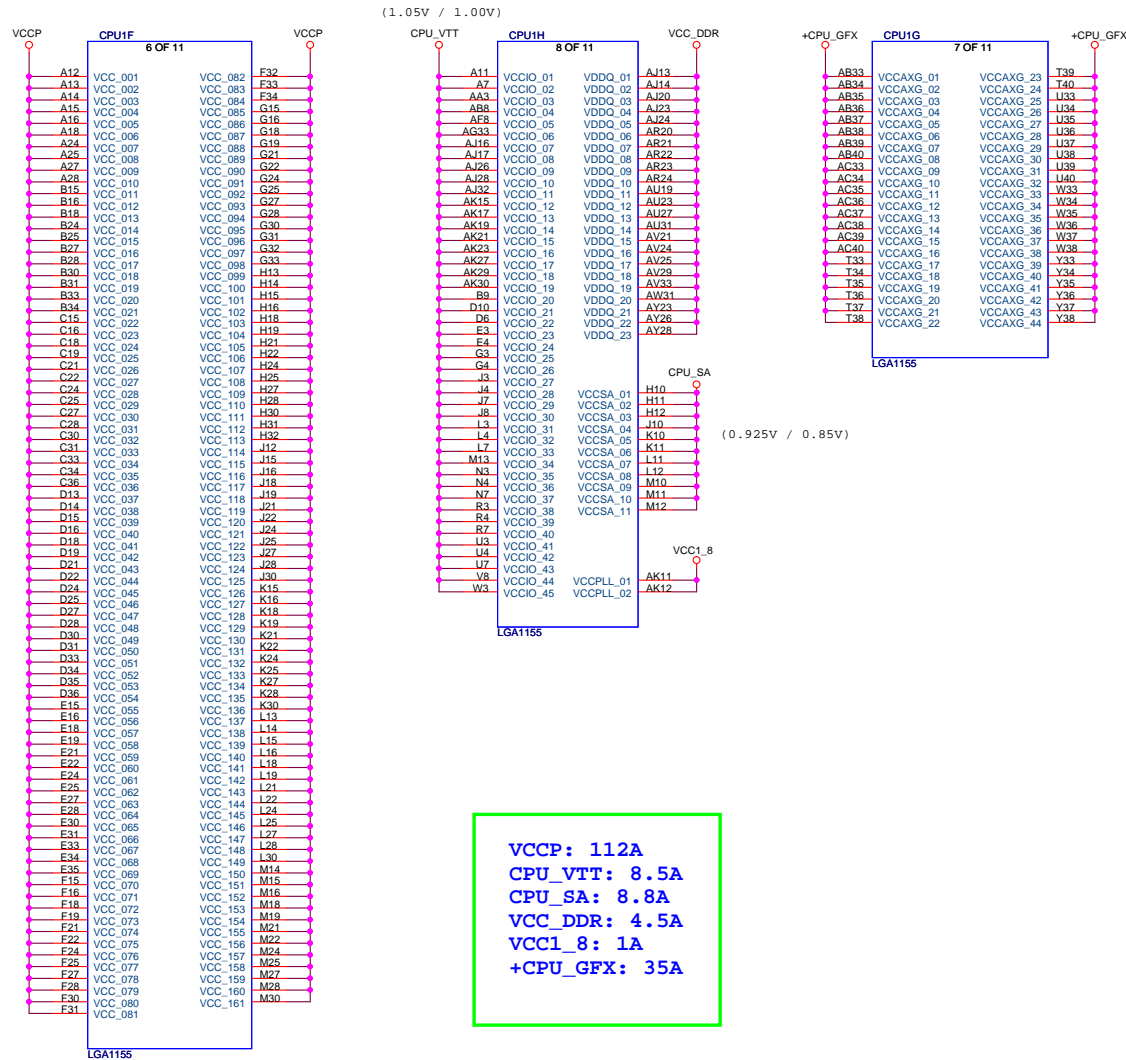
Size
Custom

Document Description
CPU-Memory

Rev	0A
-----	----

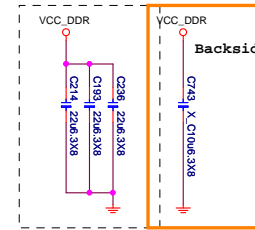
Date: Friday, May 11, 2012

Sheet 4 of 41



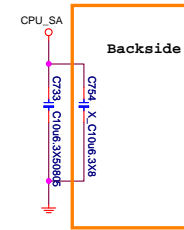
+1.5V_DDR3-Decoupling

CPU SOCKET CAVITY CAPS



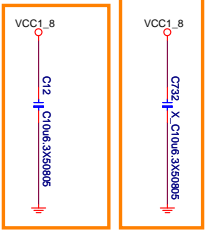
+CPU_SA Decoupling

Backside



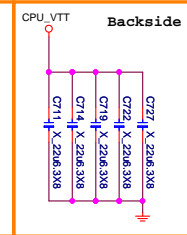
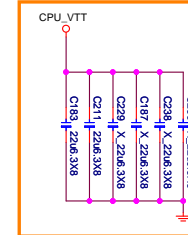
+VCC1_8 Decoupling

Backside



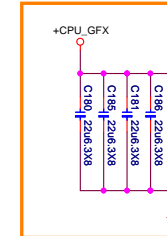
+CPU_VTT Decoupling

CPU SOCKET CAVITY CAPS

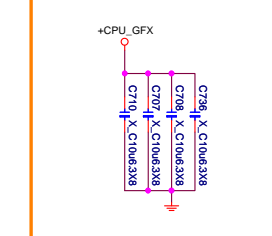


+CPU_GFX Decoupling

CPU SOCKET CAVITY CAPS

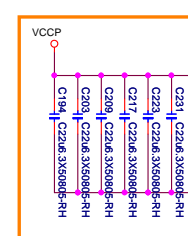


Backside

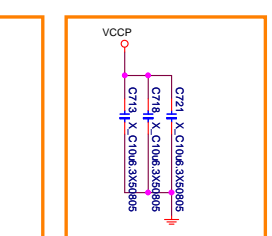


+CPU_VCCP-Decoupling

CPU SOCKET CAVITY CAPS



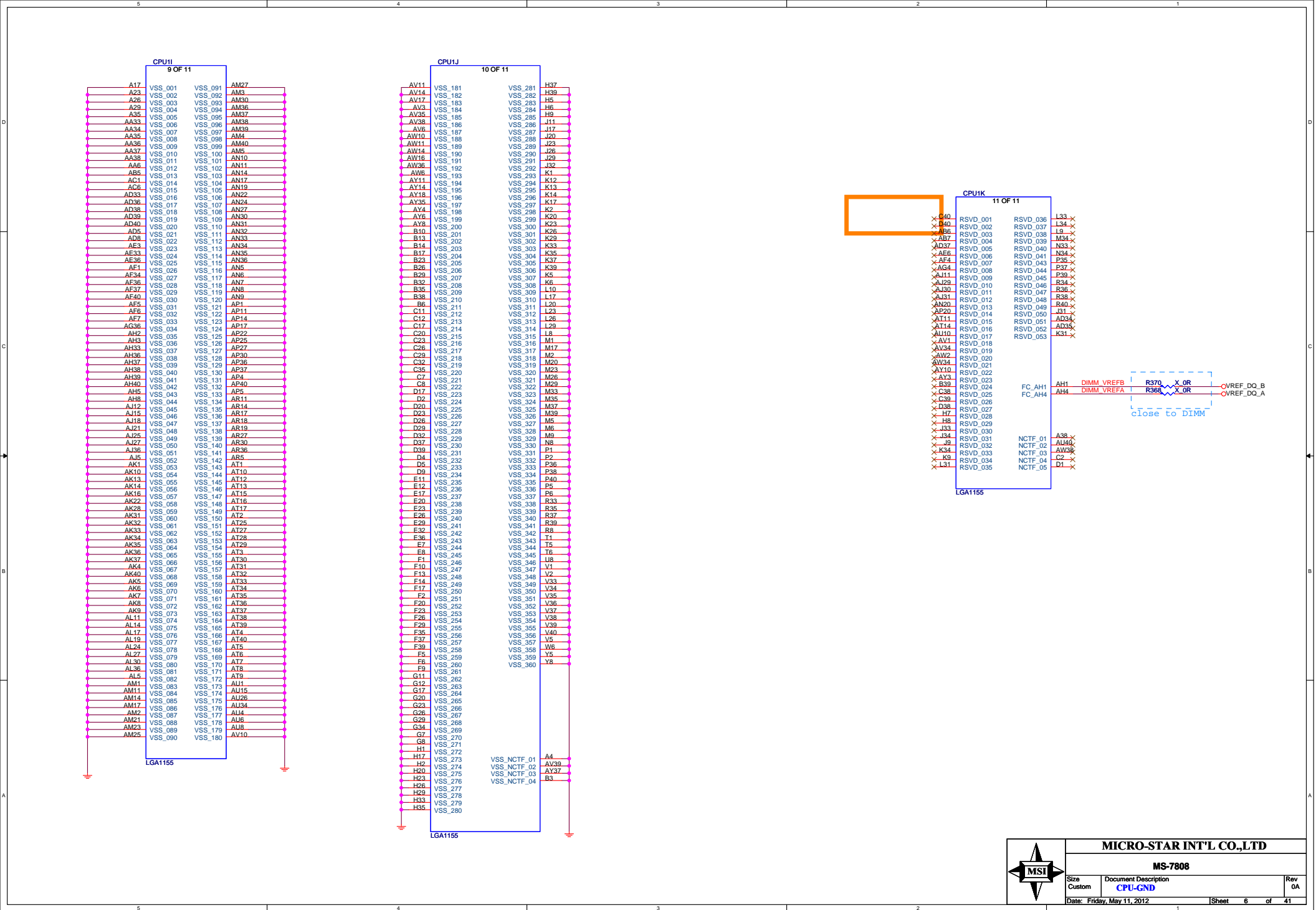
Backside



MICRO-STAR INT'L CO.,LTD

MS-7808

Size	Document Description	Rev
Custom	CPU-Power	0A
Date: Tuesday, May 15, 2012	Sheet 5 of 41	

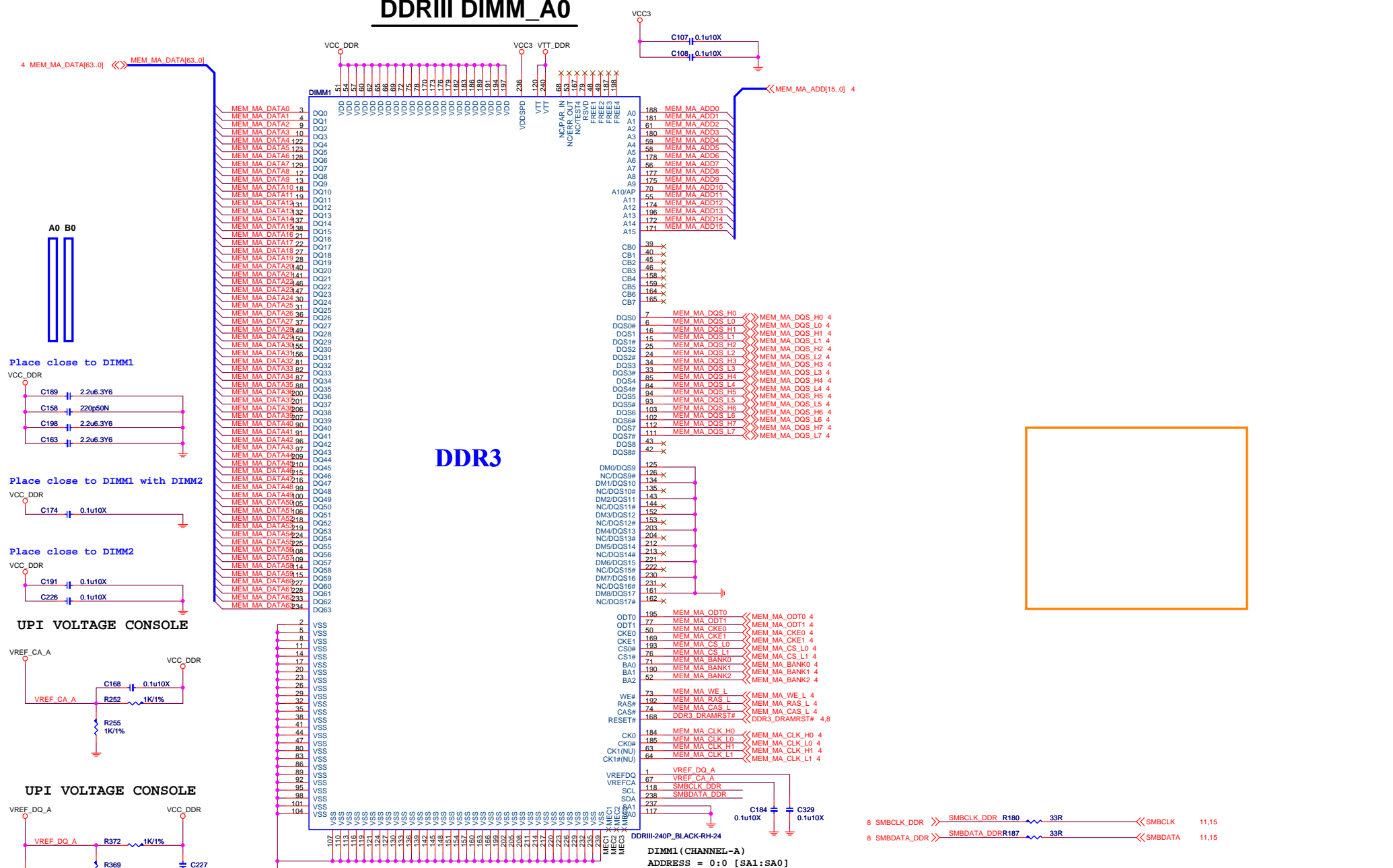


MICRO-STAR INT'L CO.,LTD

MS-7808

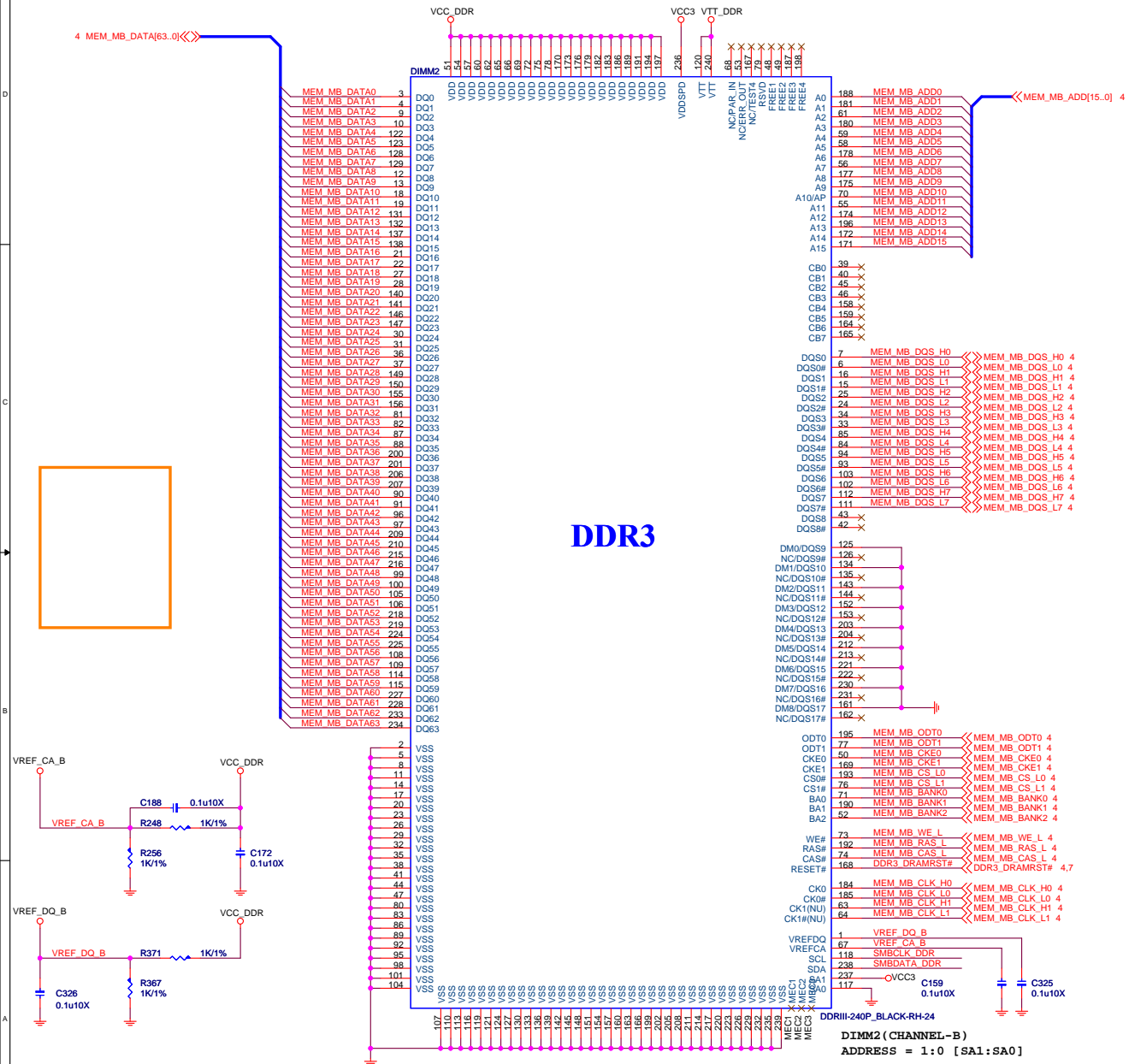
Size Custom	Document Description CPU-GND	Rev 0A
Date: Friday, May 11, 2012		
Sheet 6 of 41		

DDR3 DIMM_A0




MICRO-STAR INT'L CO.,LTD		
MS-7808		
Size Custom	Document Description DDR3 Chanet-A DIMM1/2	Rev 0A
Date: Friday, May 11, 2012		Sheet 7 of 41

DDR3 DIMM_B0

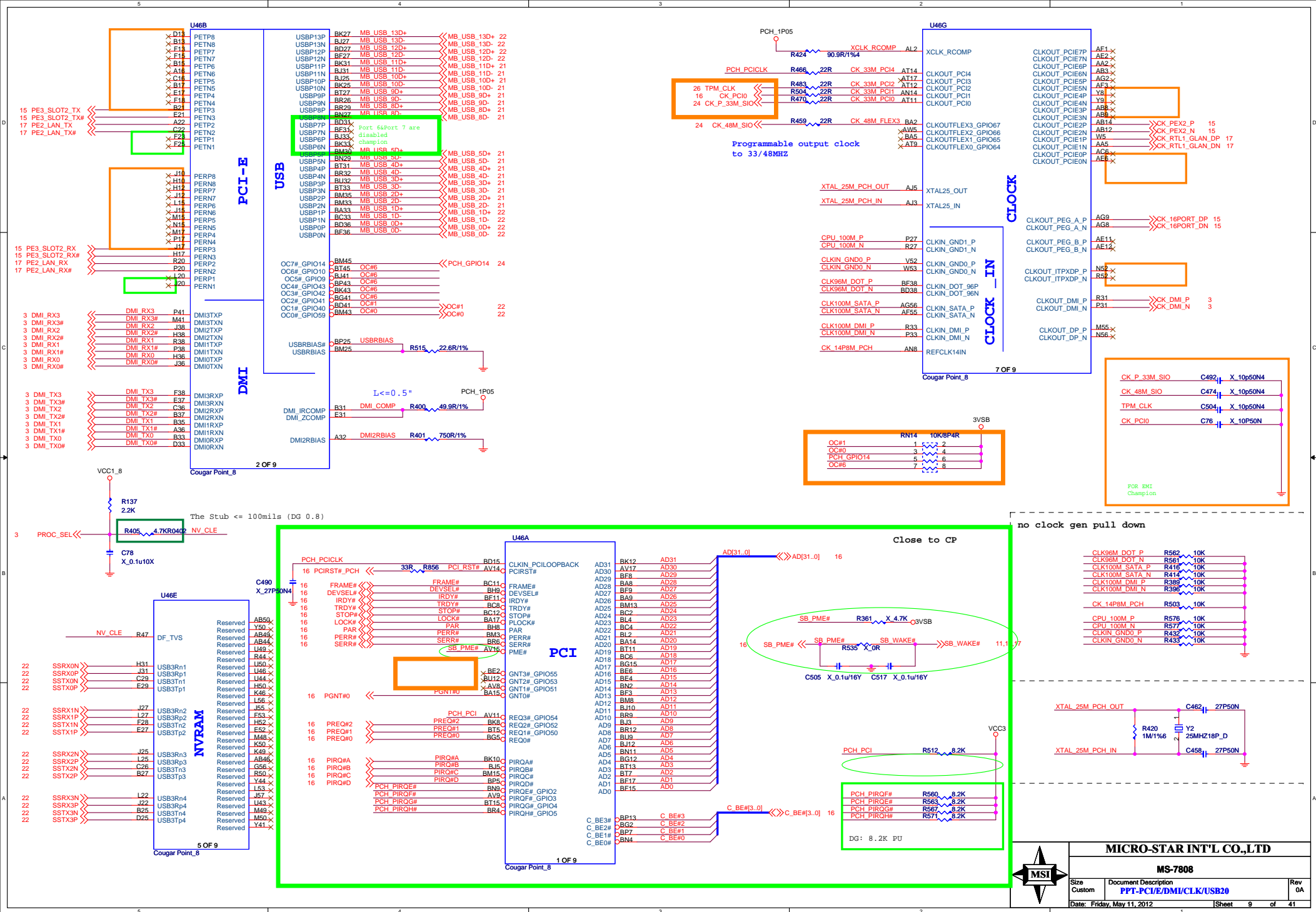


DDR3

SMBCLK_DDR << SMBCLK_DDR 7
SMBDATA_DDR << SMBDATA_DDR 7



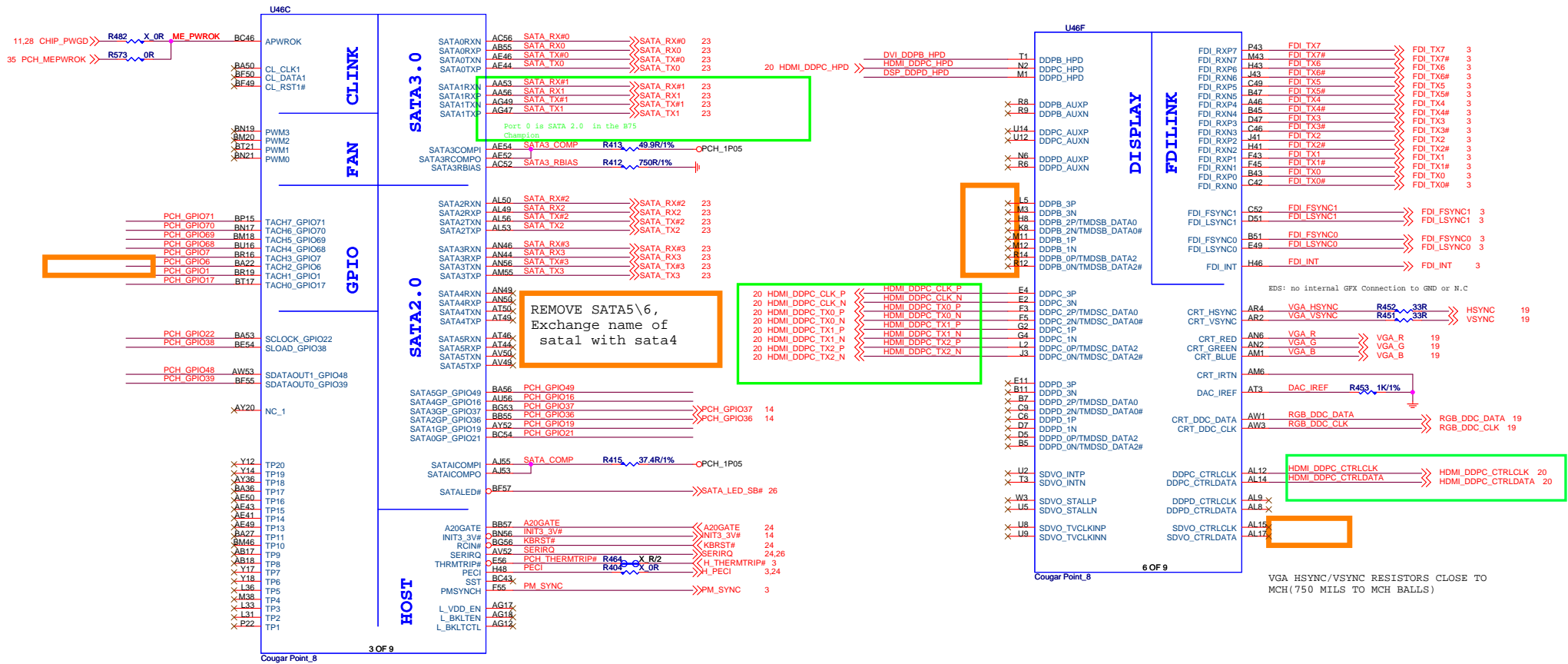
MICRO-STAR INT'L CO.,LTD		
MS-7808		
Size Custom	Document Description DDR3 Channel-B DIMM3/4	Rev 0A
Date: Friday, May 11, 2012		Sheet 8 of 41



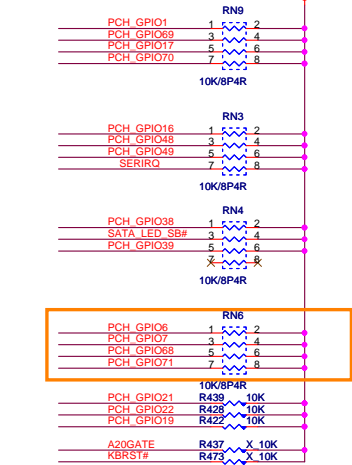
MICRO-STAR INT'L CO.,LTD

MS-7808

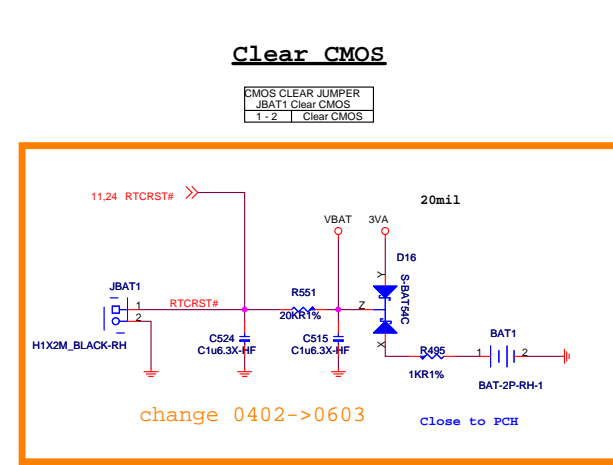
Size Custom	Document Description PPT-PCI/E/DMI/CLK/USB20	Rev 0A
Date: Friday, May 11, 2012		Sheet 9 of 41



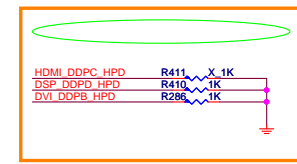
Pull HIGH for PCH



RTC and CLR_CMOS



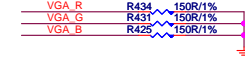
No Display port(pull down)



Enable VGA(CTRLCLK/DATA Pull High)



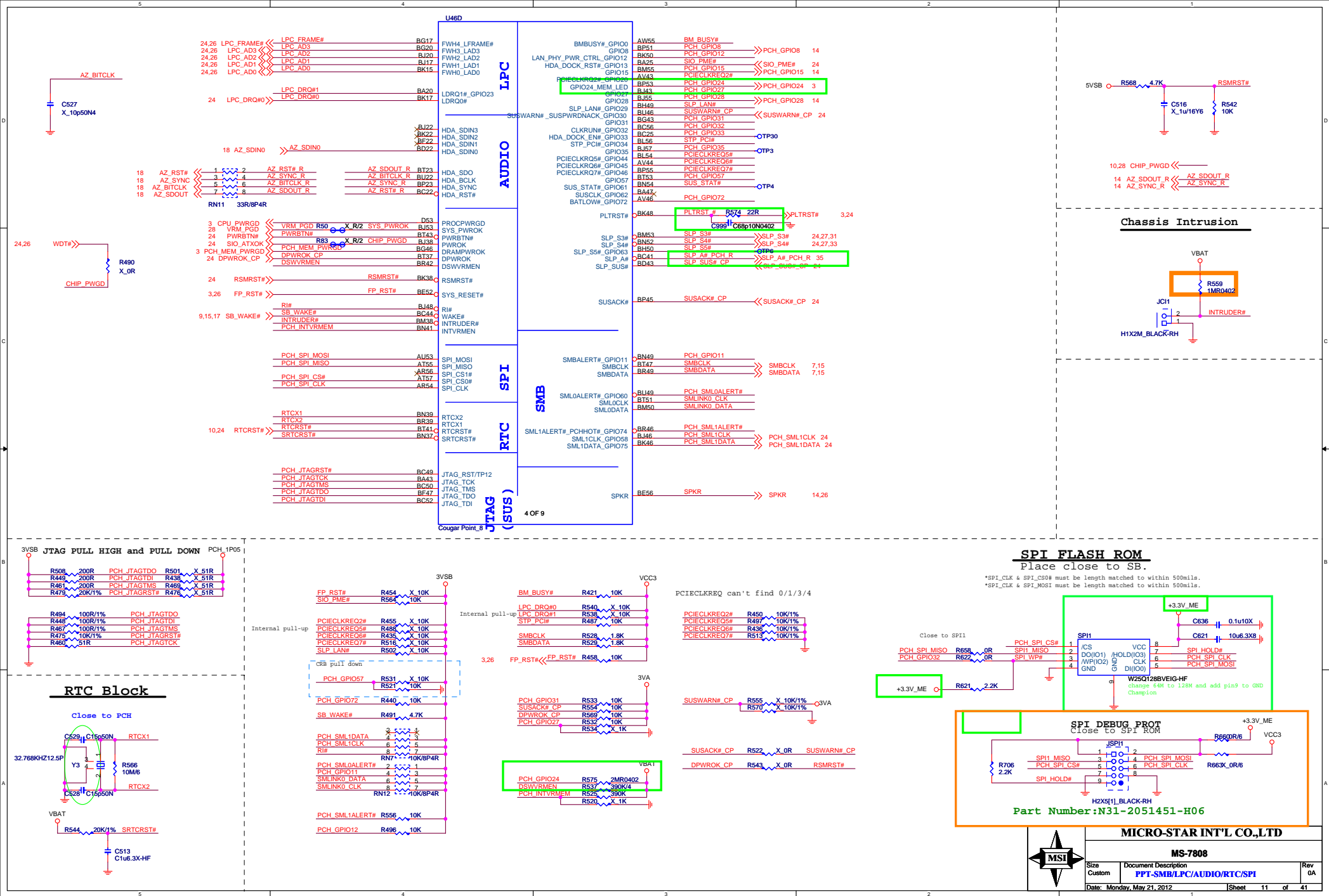
Close to PCH within 250 mils.

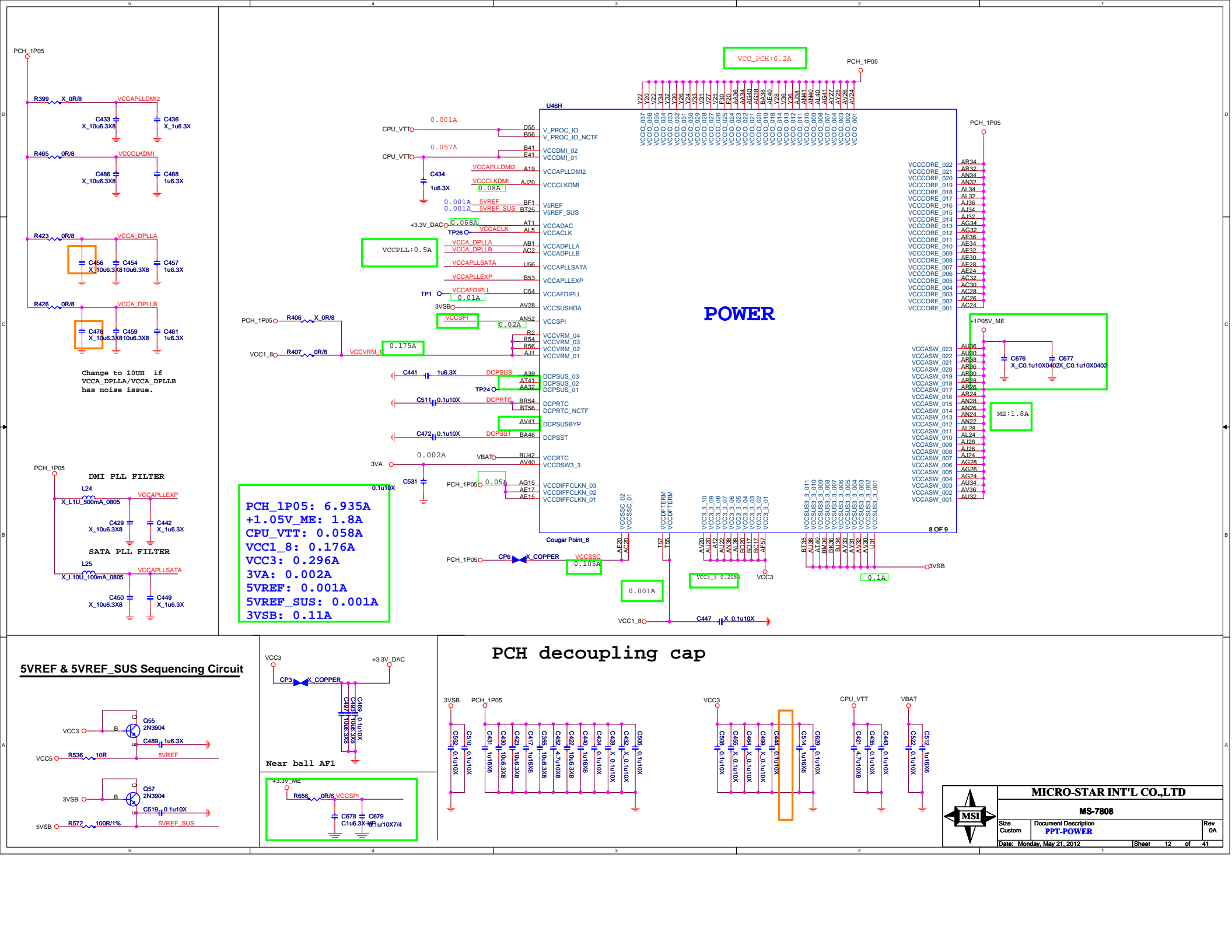


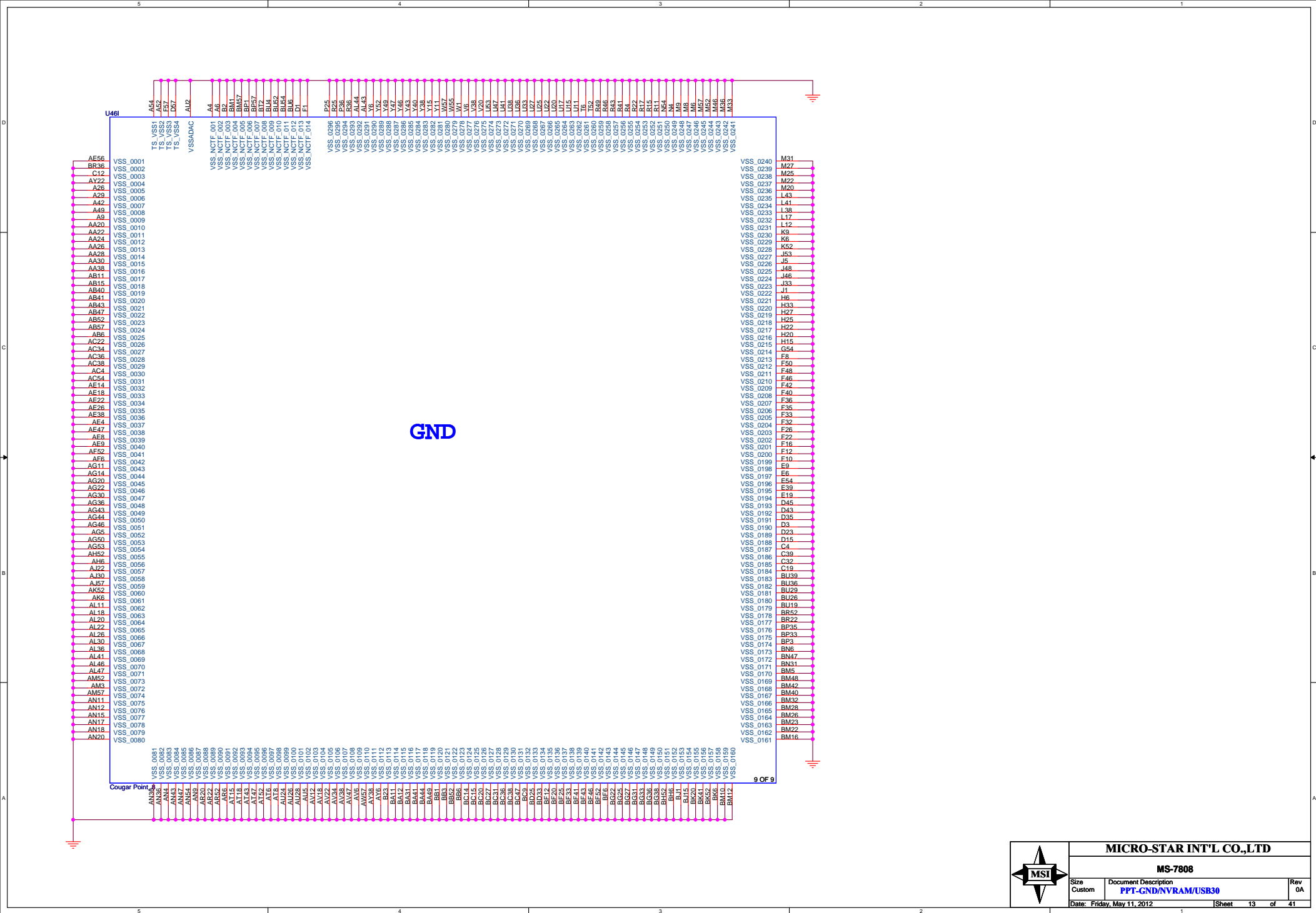
MICRO-STAR INT'L CO.,LTD

MS-7808

Size	Document Description	Rev
Custom	PPT-SATA/HOST/GPIO/VGA/CCMOS	0A
Date: Monday, May 21, 2012	Sheet 10 of 41	







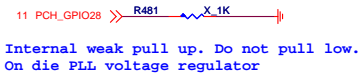
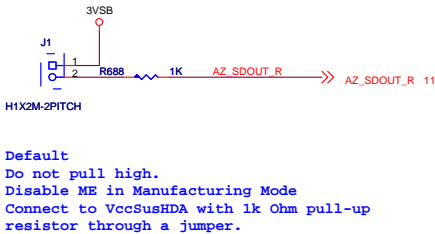
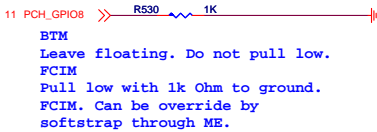
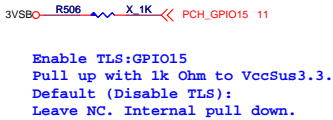
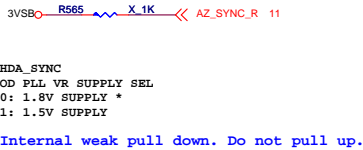
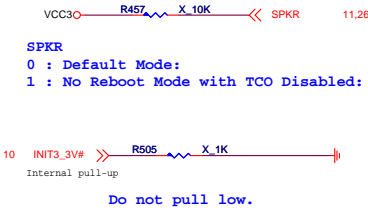
MICRO-STAR INT'L CO.,LTD

MS-7808

Size Custom	Document Description PPT-GND/NVRAM/USB30	Rev 0A
----------------	--	-----------

Date: Friday, May 11, 2012	Sheet 13 of 41
----------------------------	----------------

PCH Straps



Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:

a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3.3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.

b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window

When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.



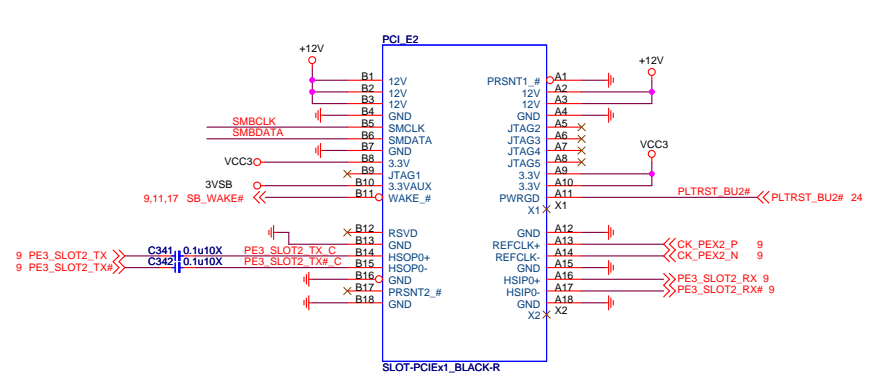
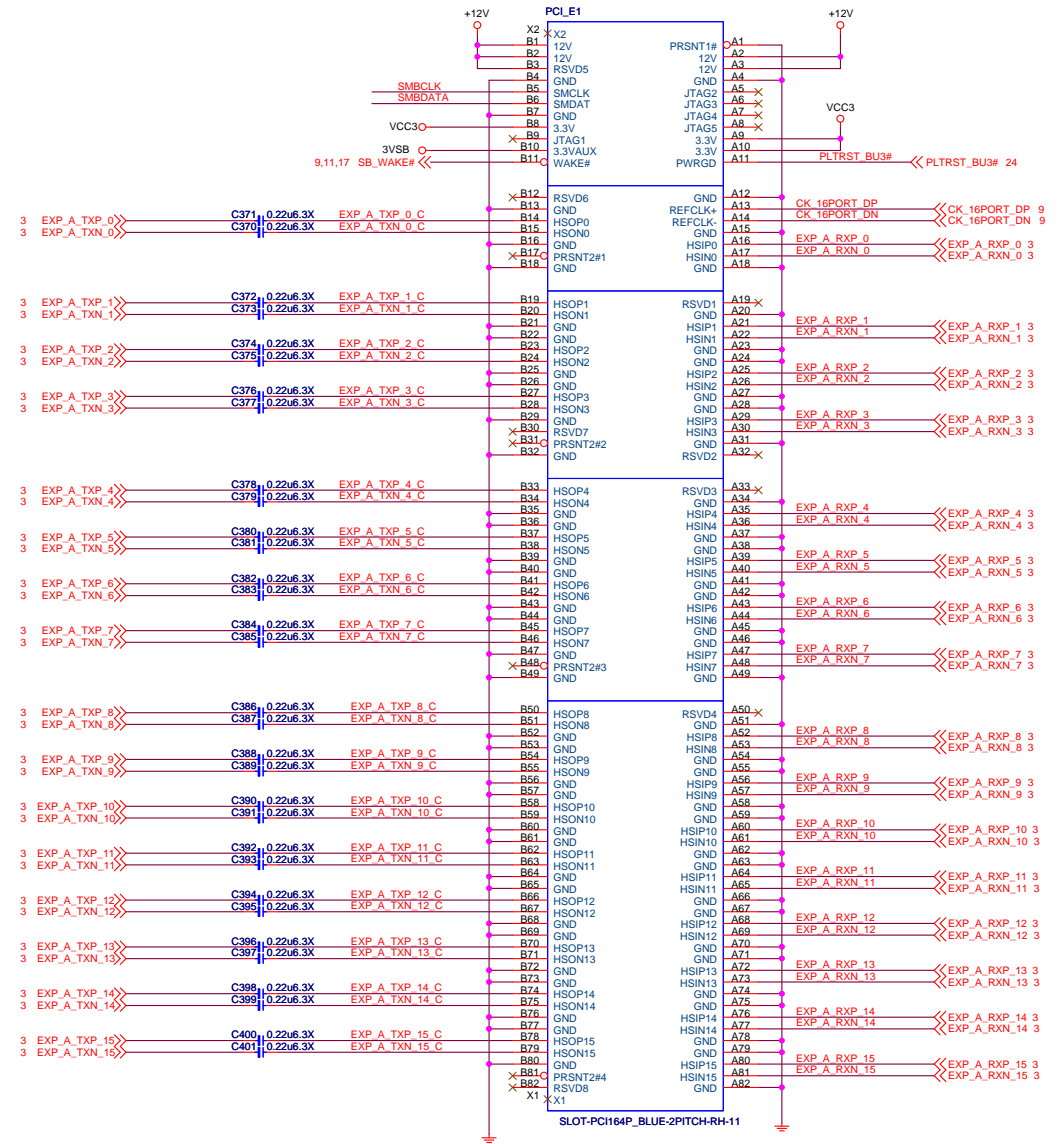
Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:

a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3.3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.

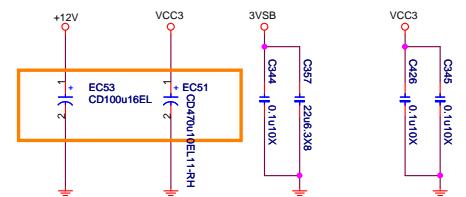
b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window

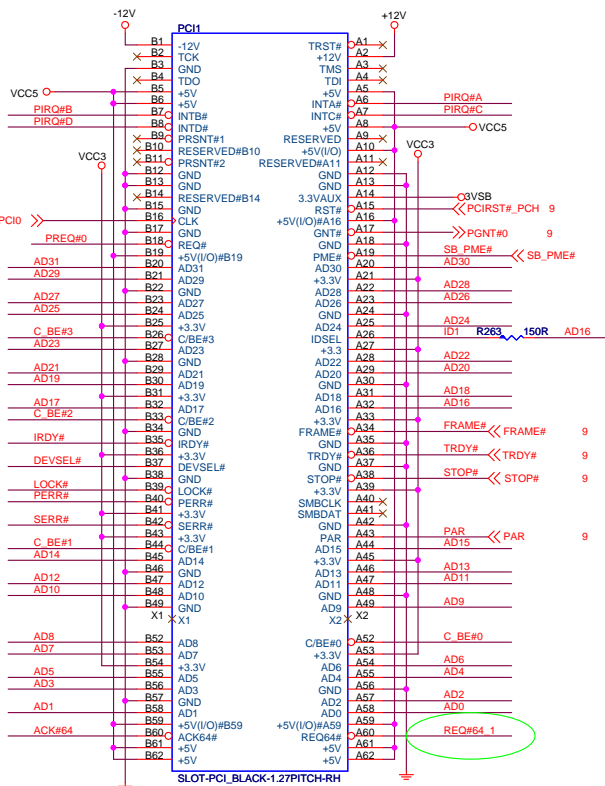
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.

7,11 SMBCLK
7,11 SMBDATA



PCE slot	
+3.3Vaux	- 375mA
+3.3V	- 9A
+12V	- 6A

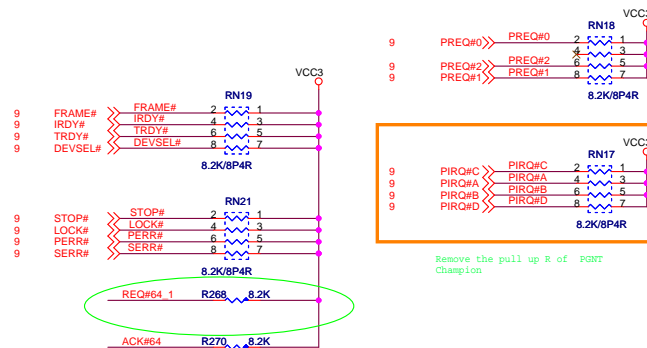
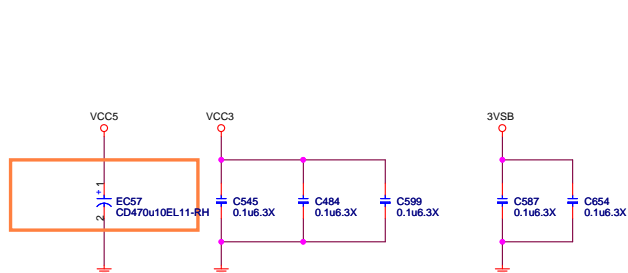




IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

AD[31..0] <<> AD[31..0] 9
 C_BE[3..0] <<> C_BE[3..0] 9

PCI PULL-UP / DOWN RESISTORS



Remove the pull up R of PGT Champion

PCI slot

+3.3Vaux	- 375mA
+3.3V	- 7.6A
+12V	- 0.5A

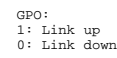
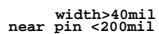


MICRO-STAR INT'L CO.,LTD

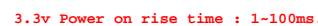
MS-7808

Size Custom	Document Description	Rev 0A
	PCI Slots	
Date: Friday, May 11, 2012	Sheet 16	of 41

near

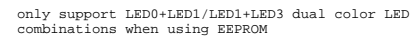
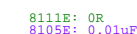
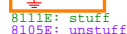


Pin49: 9 via from top layer to GND layer
and make the via at the center of IC.

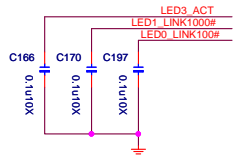


8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13



LAN Connector



Giga-Lan		10/100-Lan	
N58-22F0731 Link Yellow Active Blinking 1000 Orange 100 Green 10 None		N58-22F0771 Link Yellow Active Blinking 100 Green 10 None	
19		19	
20		20	
Orange			
21		21	
22		22	

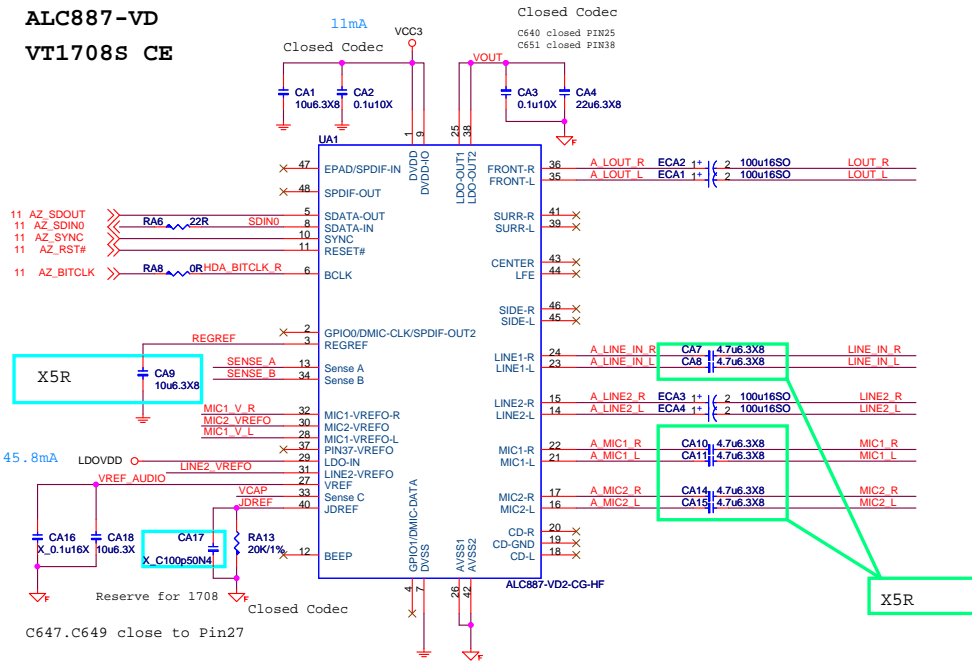


MICRO-STAR INT'L CO., LTD.

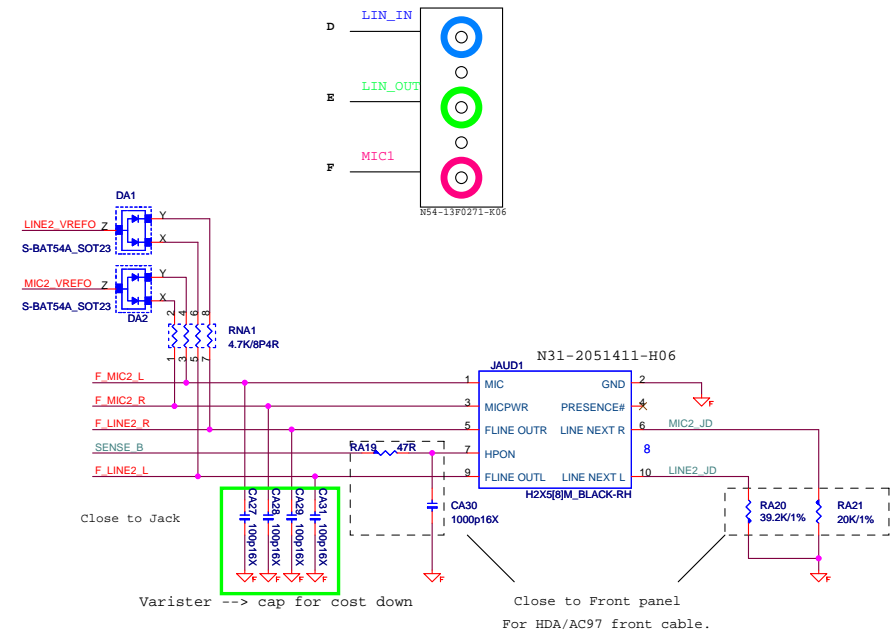
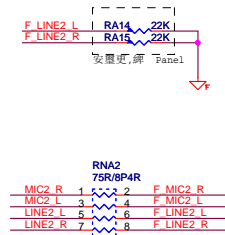
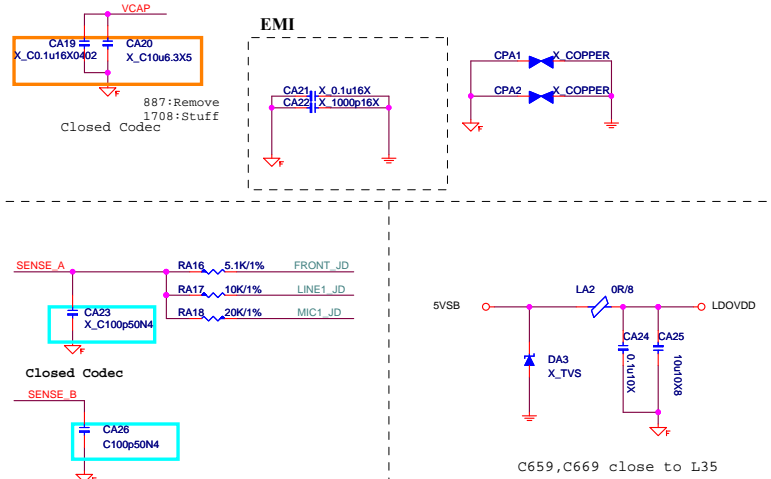
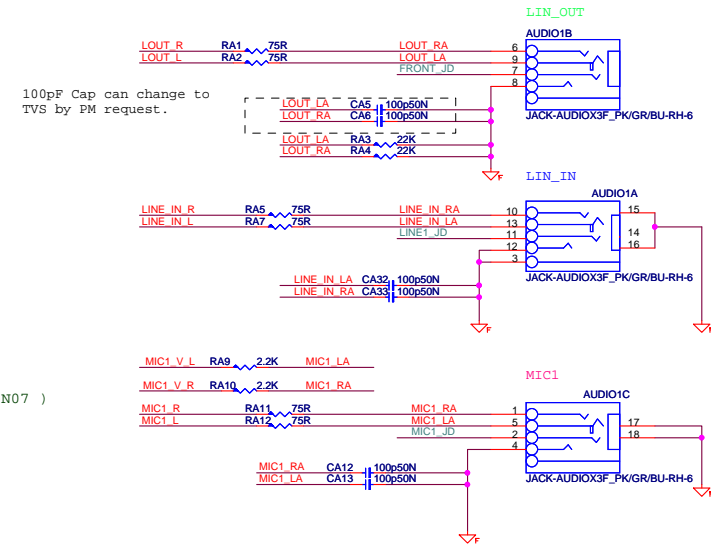
MS-7808

Size Custom	Document Description LAN-RTL8111E/8105E	Rev 0A
Date: Friday, May 11, 2012	Sheet 17 of 41	

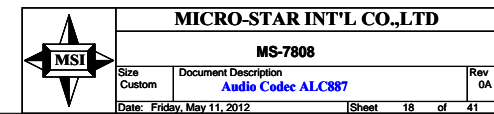
ALC887-VD
VT1708S CE



EL 100u (C94-1012511-N07)



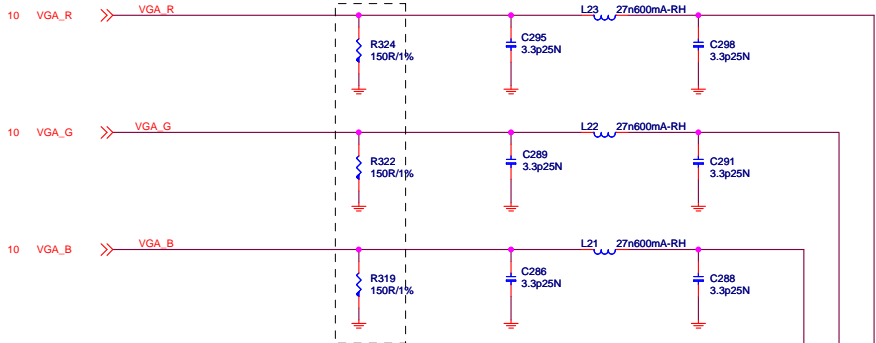
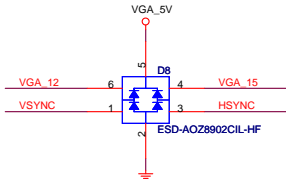
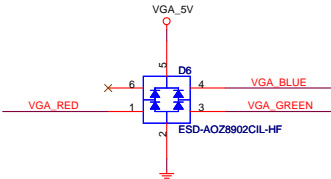
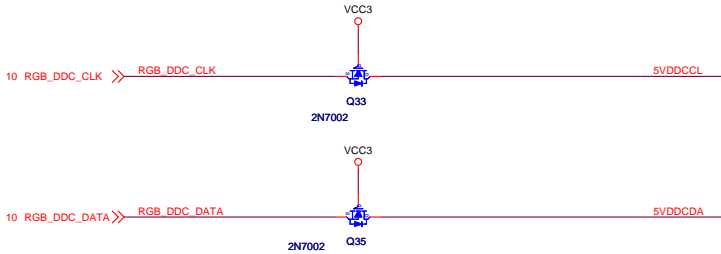
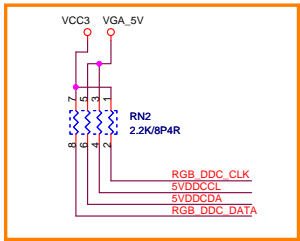
SPDIF OUT



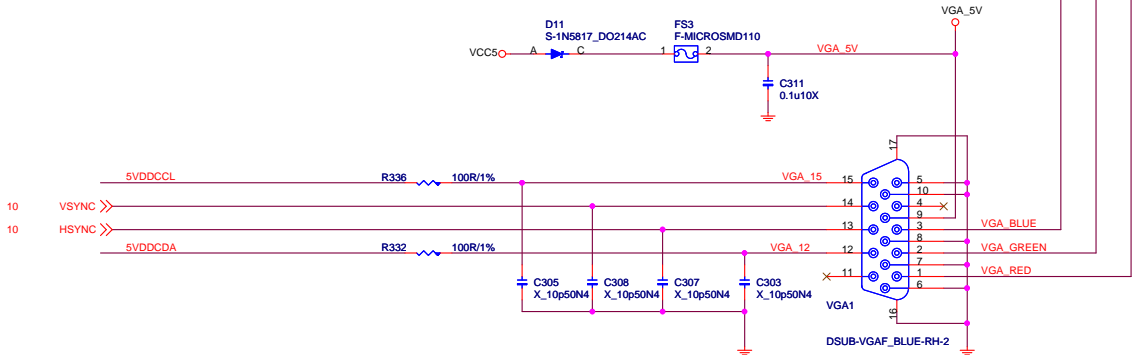
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift



PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN

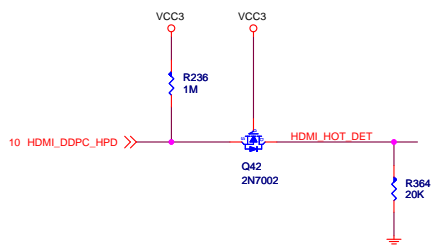
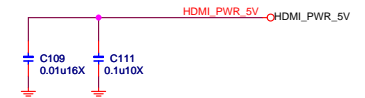
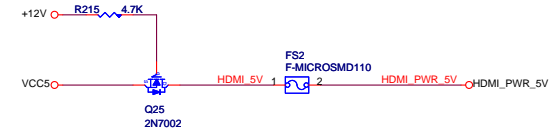
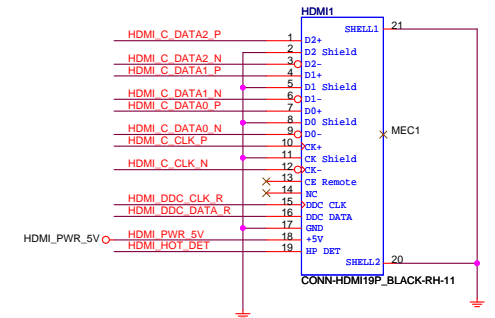
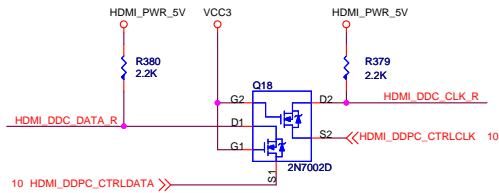
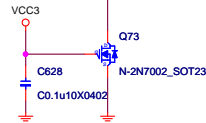
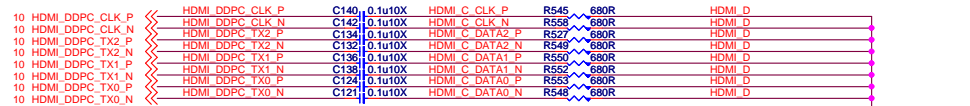


MICRO-STAR INT'L CO.,LTD

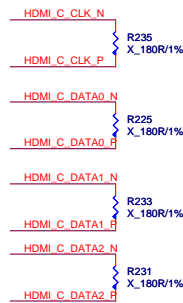
MS-7808

Size Custom	Document Description VGA Connector	Rev 0A
Date: Friday, May 11, 2012	Sheet 19 of 41	

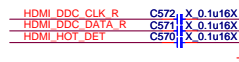
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



For EMI



EMI



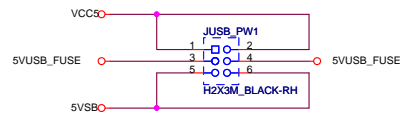
MICRO-STAR INT'L CO.,LTD

MS-7808

Size Custom Document Description HDMI Connector Rev 0A

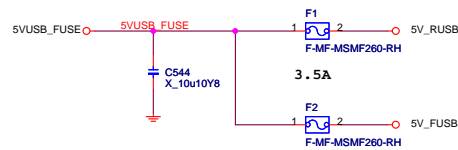
Date: Friday, May 11, 2012 Sheet 20 of 41

5V_RUSB Switch

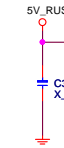
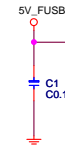
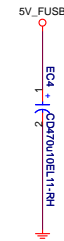
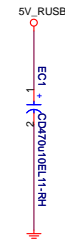


Default VCC5 (PIN1-3,2-4)

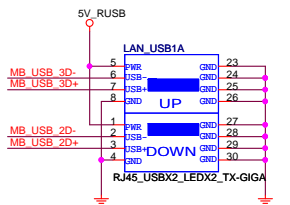
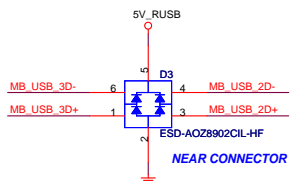
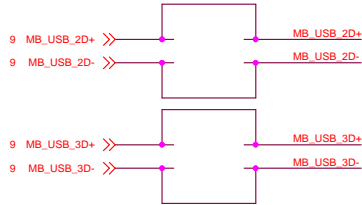
5V_RUSB must 120mm



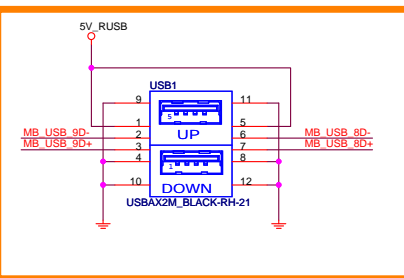
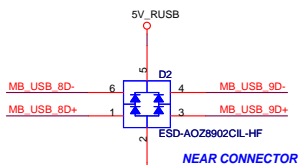
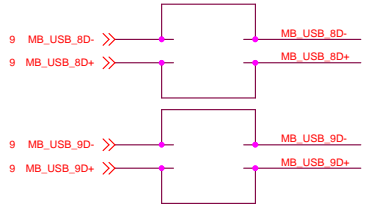
JUSB_PW1	BIOS Menu	Wake up support
1-3,2-4	EUP Enable	Not support
	EUP Disable	Not support
3-5,4-6	EUP Enable	Not support
	EUP Disable	support



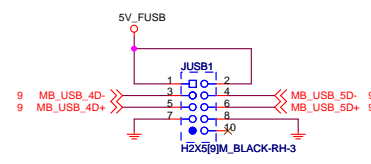
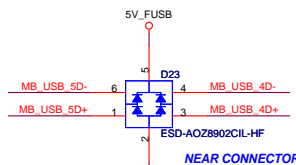
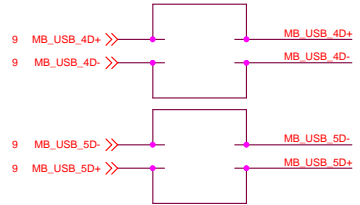
REAR USB PORT 8,9 (With LAN)



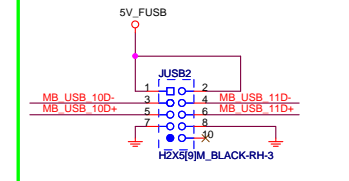
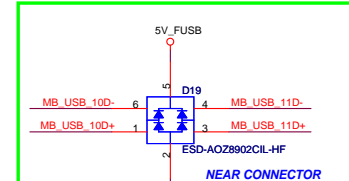
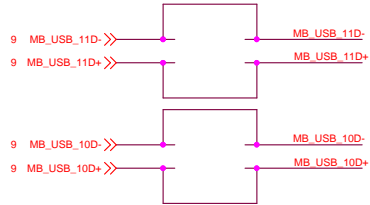
REAR USB PORT 8,9 (USB1)



FRONT USB PORT 0,1



FRONT USB PORT 8,9



Remove USB2.0 PORT 10,11
USB6&USB7
Champion

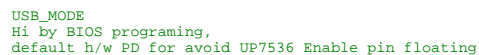


MICRO-STAR INT'L CO.,LTD

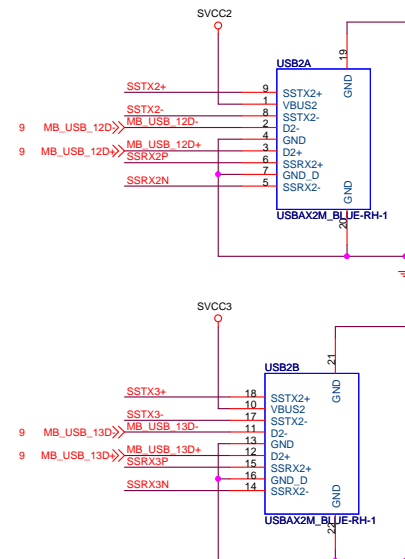
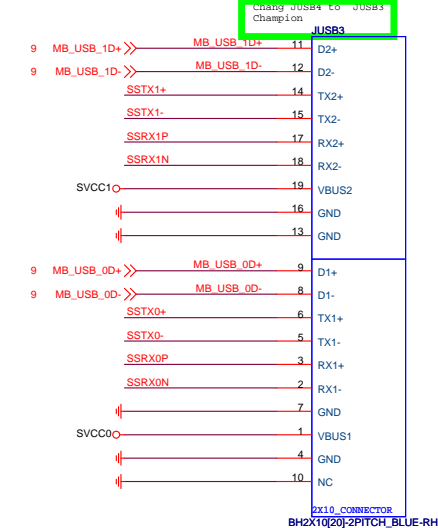
MS-7808

Size	Document Description	Rev
Custom	Rear I/O & USB2.0 Connector	0A
Date: Wednesday, May 23, 2012	Sheet 21 of 41	

Same as SLP S3#



USB MODE States				
MODE	G3	S4/S5	S0	S3
EUP Disable	0	0	1	1
EUP Enable	0	0	1	1



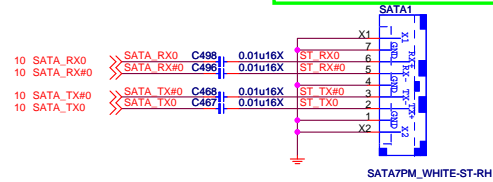
MS-7808

Size Custom	Document Description USB3.0 Connector	Rev 0A
Date: Monday, May 21, 2012		Sheet 22 of 41

Change SATA5G PORT0,1 to SATA PORT 0

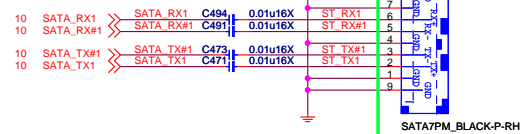
SATA 6G PORT 0

3.0 white



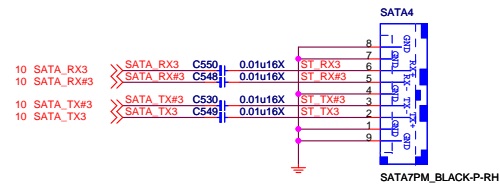
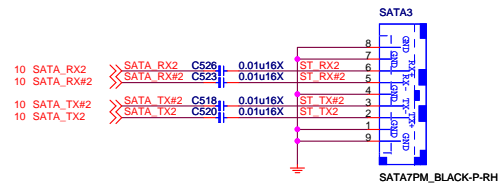
add SATA 3G PORT 1
Champion

SATA 3G PORT 1



change SATA3.0 to SATA 2.0
Champion

SATA 3G PORT 2,3



REMOVE SATA5\6 , Exchange name of satal with sata4



MICRO-STAR INT'L CO.,LTD

MS-7808

Size
Custom

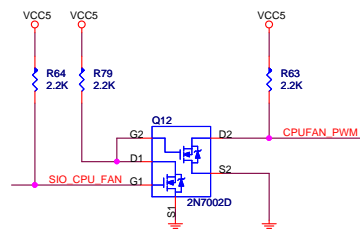
Document Description
SATA Connector

Date: Friday, May 11, 2012

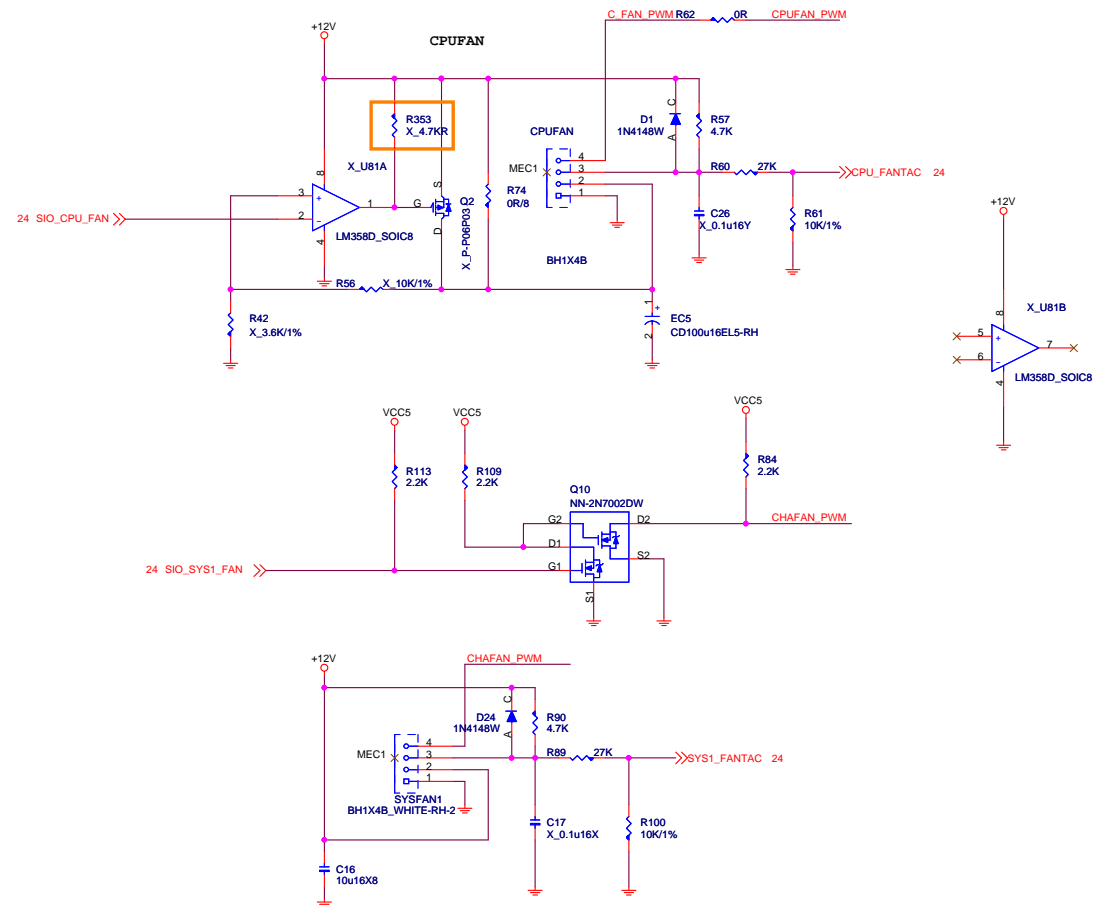
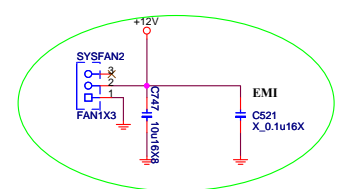
Rev
0A

Sheet 23 of 41

FAN-COUNTROL CIRCUIT

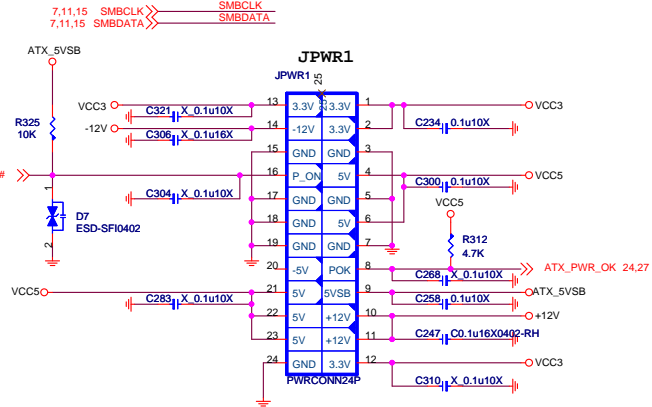


SYSTEM FAN1

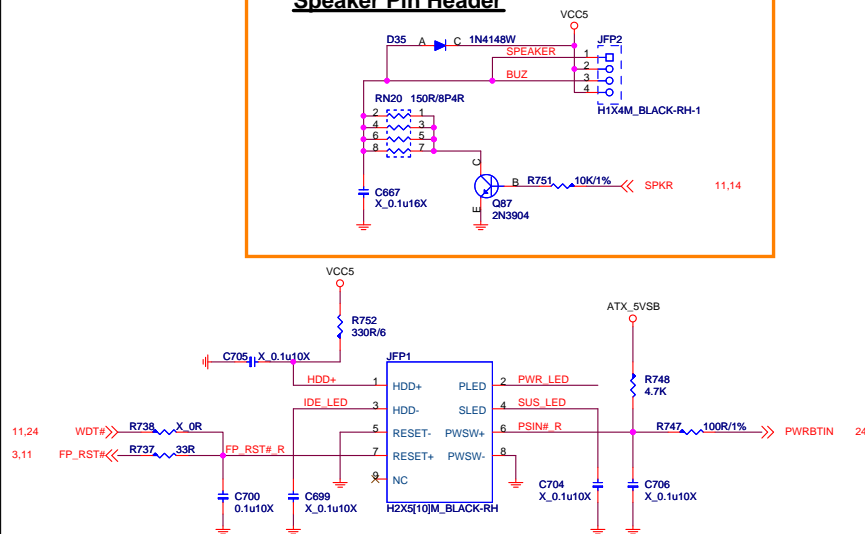


MICRO-STAR INT'L CO.,LTD		
MS-7808		
Size	Document Description	Rev
Custom	FAN Control	0A
Date: Friday, May 11, 2012	Sheet 25 of 41	

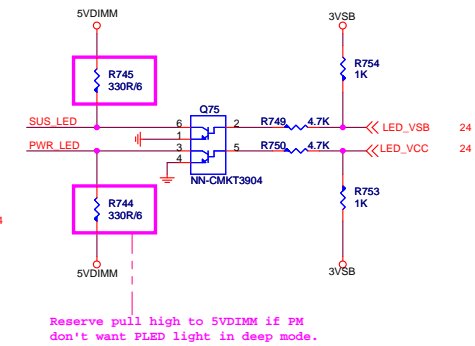
ATX POWER CONNECTOR



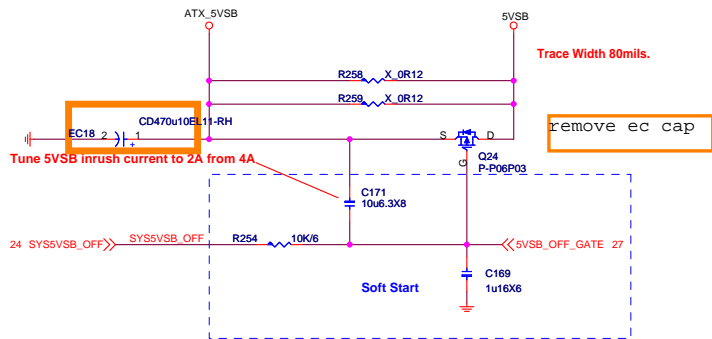
Speaker Pin Header



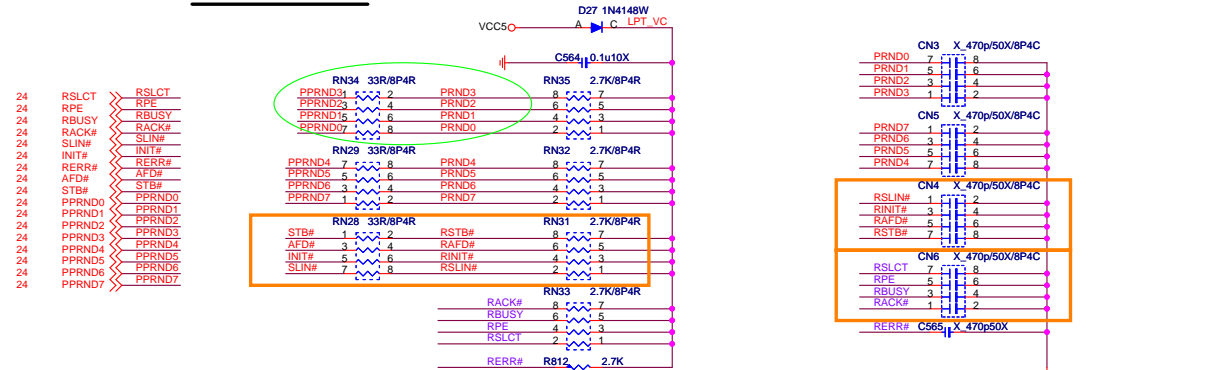
LED (for Fintek 71869)



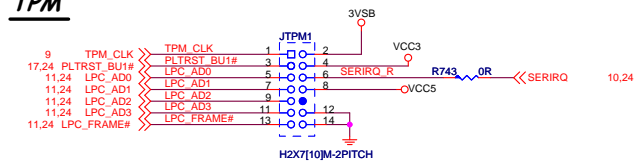
5VSB Power Switch



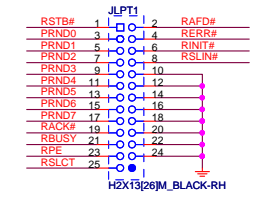
PARALLAL PORT



TPM

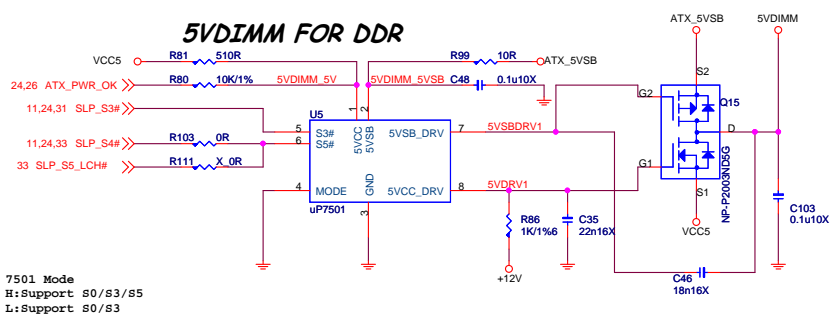


REMOVE Turbo Button

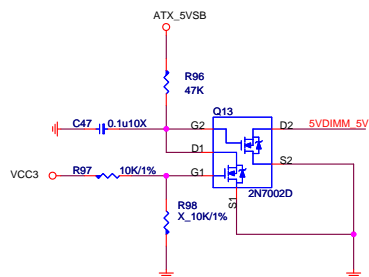
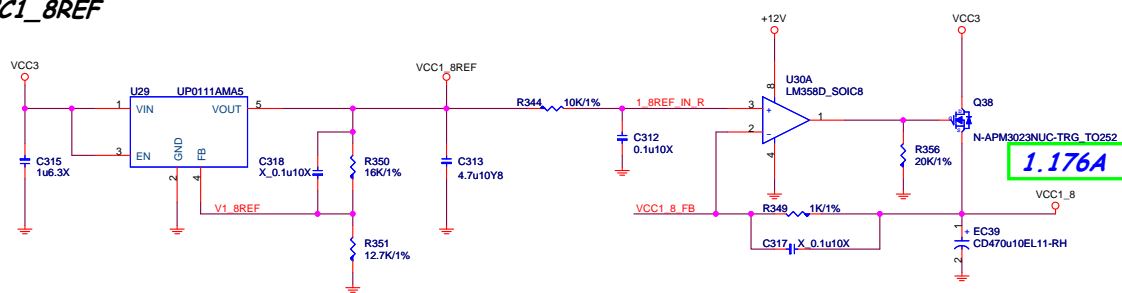


N31-2131151-H06 : 2.0mm
N31-2131131-H06 : 2.54mm

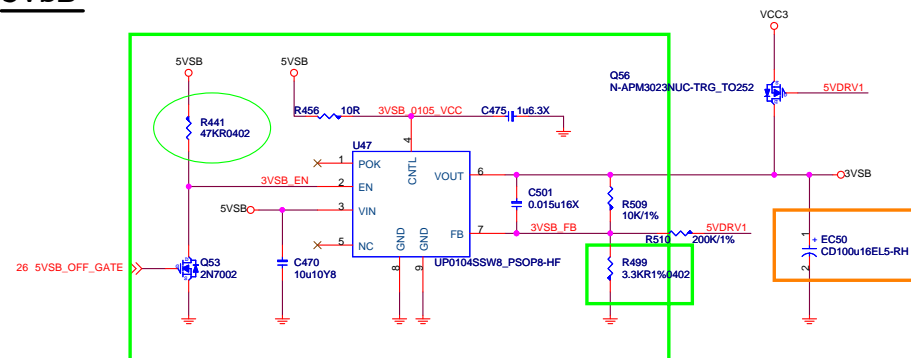
5VDIMM FOR DDR



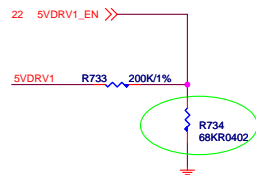
VCC1_8REF



3VSB

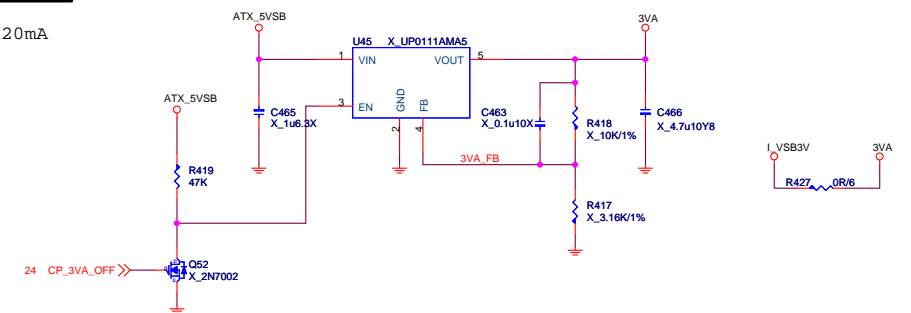


USB MODE



3VA

20mA

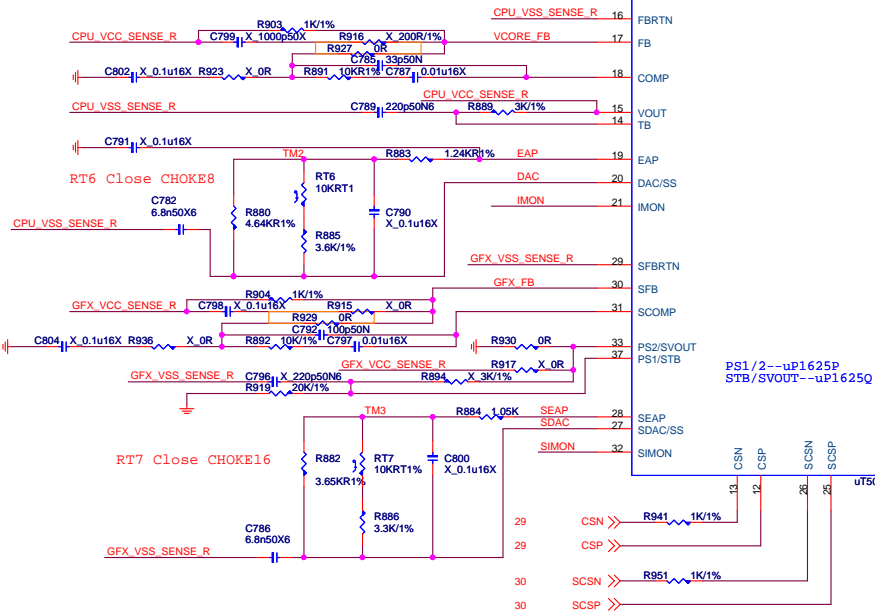
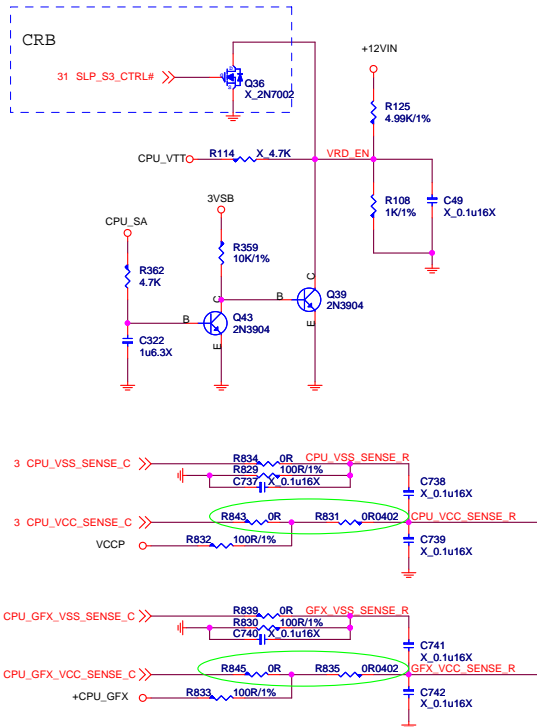
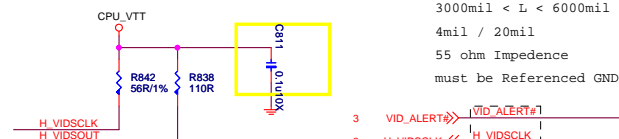
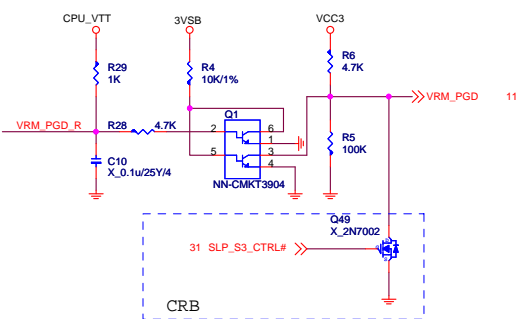


MICRO-STAR INT'L CO.,LTD

MS-7808

Size	Document Description	Rev
Custom	ACPI controller UPI	0A
Date: Friday, May 11, 2012	Sheet 27 of 41	

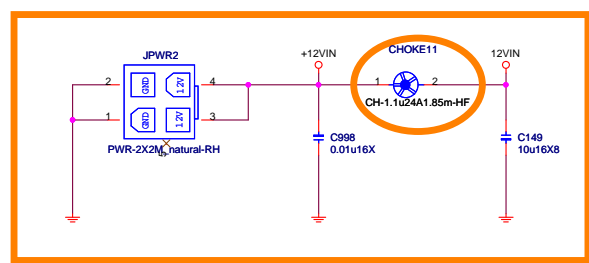
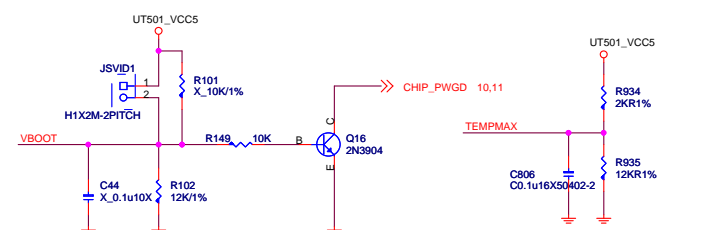
VRMPWRGD LEVEL SHIFT



UPI VOLTAGE CONSOLE

0x20: RH=10K, RL=OPEN

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (Kohm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

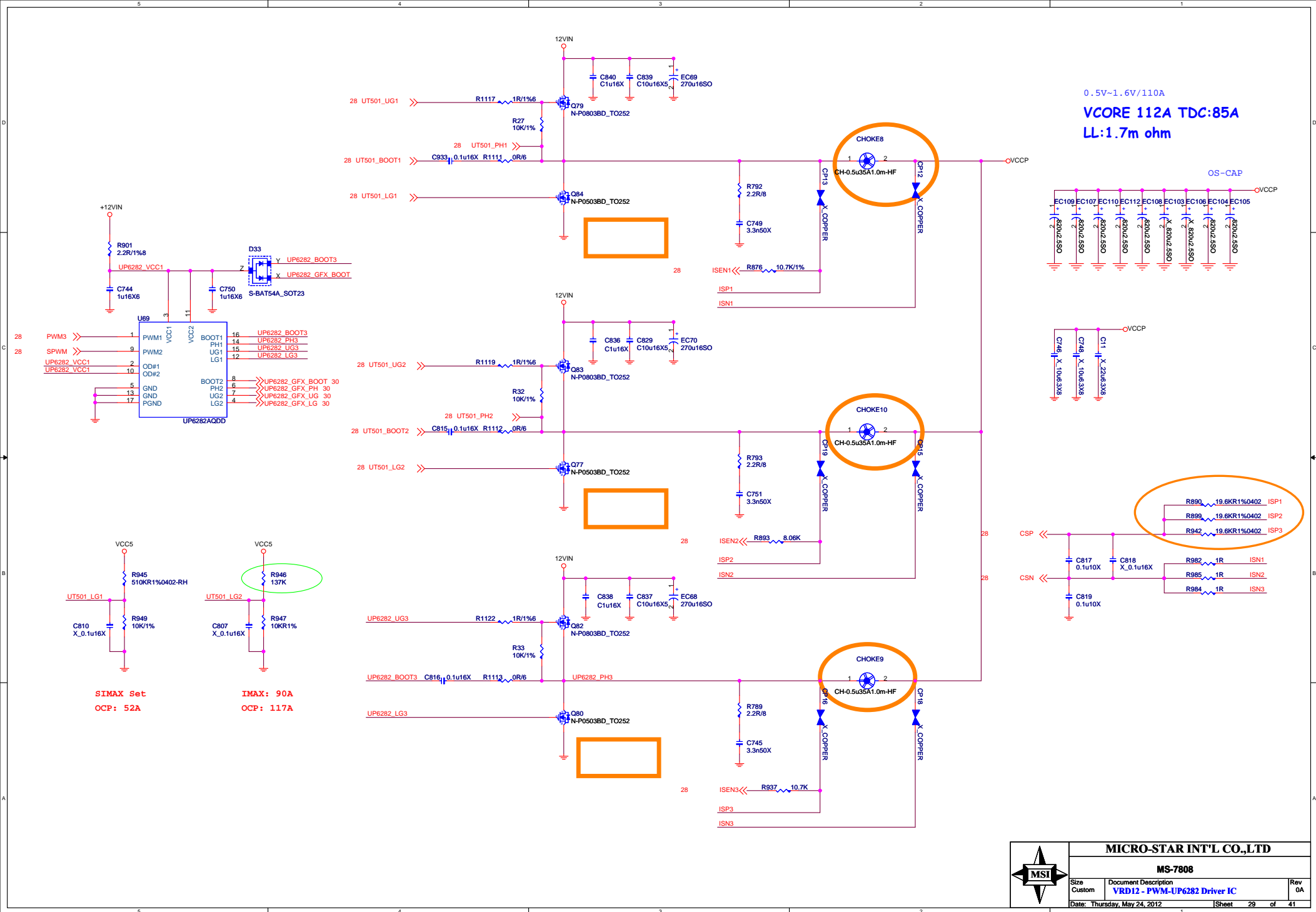


MICRO-STAR INT'L CO.,LTD

MS-7808

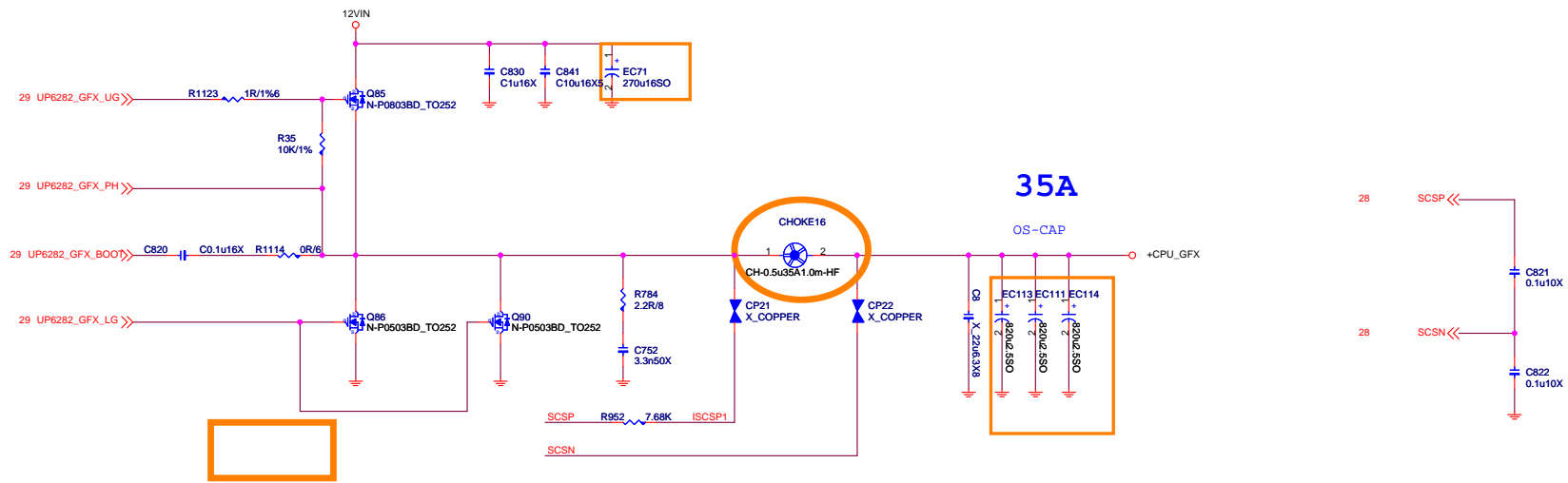
Size Custom Document Description VRD12 - PWM-UT501 Rev 0A

Date: Tuesday, May 22, 2012 Sheet 28 of 41



CPU_GFX:0.25-1.52

35A FOR CPU



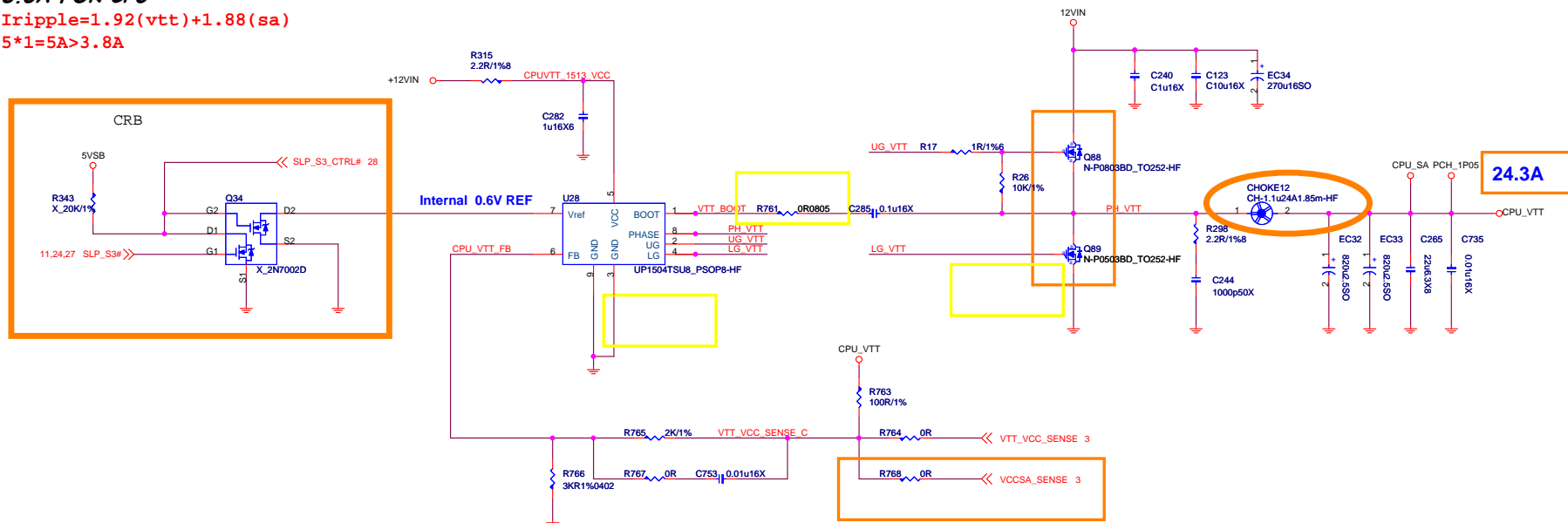
CPU_VTT:1.05/1.00 MAX 24.3A

CPU VTT 8.5A SA Core =8.8A PCH Core =7A

8.5A FOR CPU

$\text{Irripple} = 1.92(\text{vtt}) + 1.88(\text{sa})$

$5 \times 1 = 5\text{A} > 3.8\text{A}$

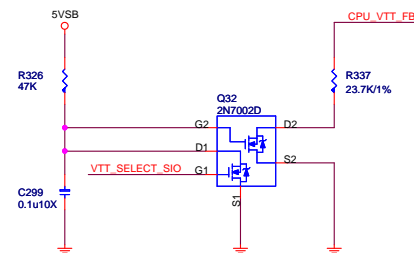


VTT_SELECT
0 : 1.0V
1 : 1.05V

suggest 1.5V
max : 1.8V

VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V



MICRO-STAR INT'L CO.,LTD

MS-7808

Size	Document Description	Rev
Custom	VTT POWER- uP1513- 1Phase MOS	0A
Date: Monday, May 21, 2012		Sheet 31 of 41

CPU_SA:0.925/0.85

SA Core =8.8A

			MICRO-STAR INT'L CO.,LTD		
			MS-7808		
Size	Document Description			Rev	
Custom	CPU_SA OP+MOS 1-Phase			0A	
Date: Friday, May 11, 2012			Sheet	32	of 41

DDR Power:1.5V

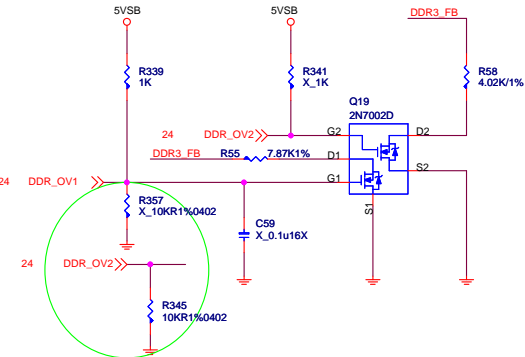
DDR3_1.5V 4.75A+5.5A+0.5A=10.75A

4.75A FOR CPU

5.5A FOR 2DIMM

0.5A FOR DDR VTT

DDR OV

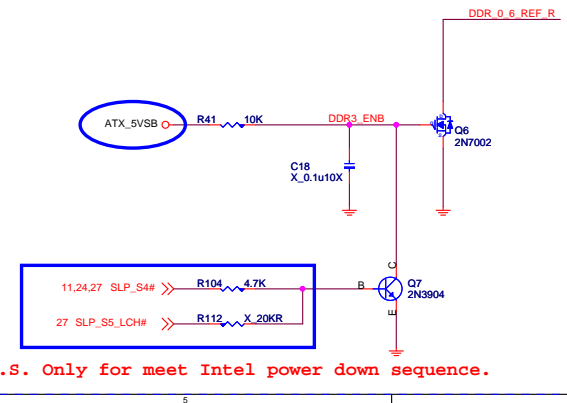


*Default 1.5V

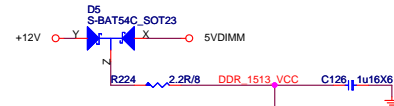
DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01(S/IO)

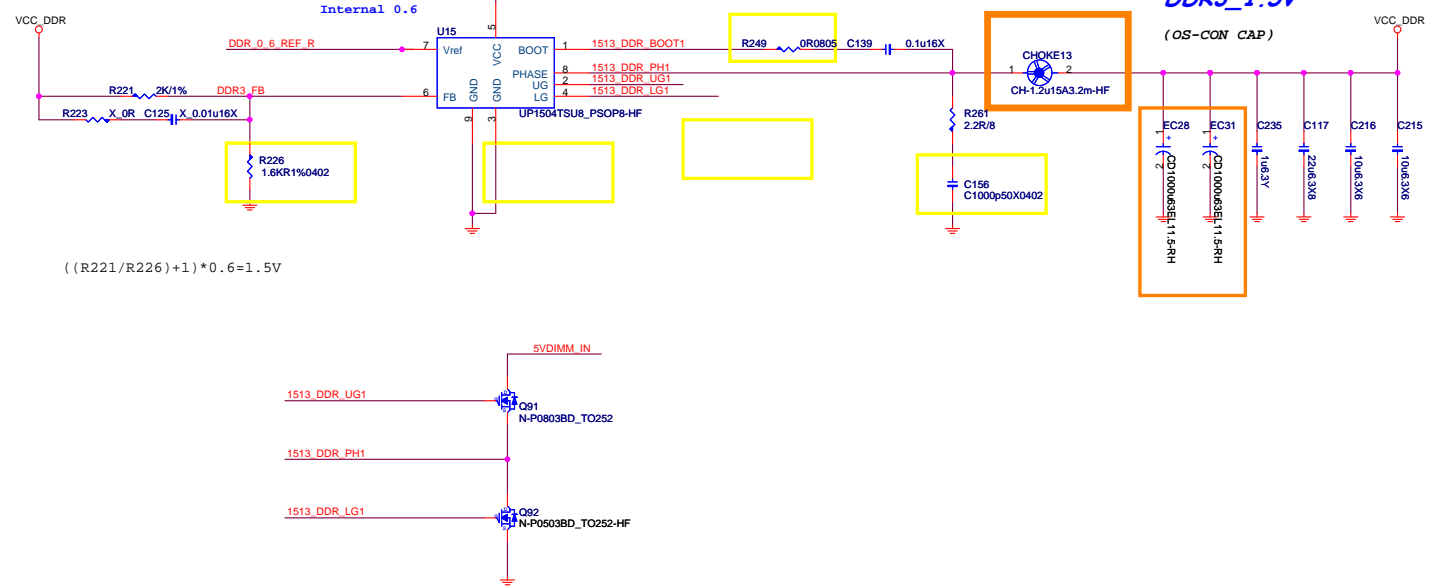
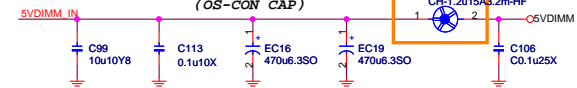
DDR_OV2 = GPIO02(S/IO)



P.S. Only for meet Intel power down sequence.



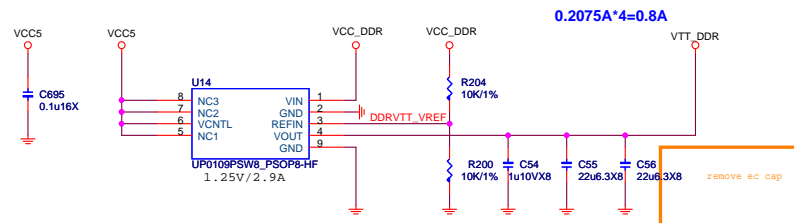
Tripple=8A
4.7*2*1=9.4A>8A



$$((R221/R226)+1)*0.6=1.5V$$

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

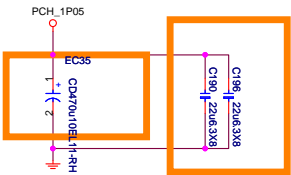


MICRO-STAR INT'L CO.,LTD

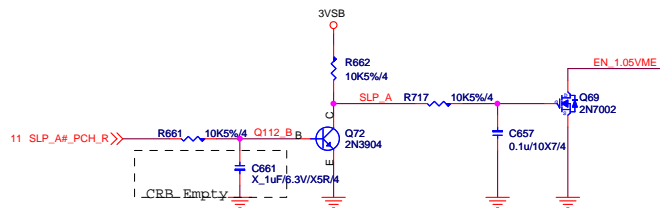
MS-7808

Size	Document Description	Rev
Custom	DDR Power -UP1513 1-Phase MOS	0A
Date: Friday, May 18, 2012	Sheet 33 of 41	

PCH Power:1.05V
PCH Core 6.2A+0.105A+0.5A+0.08A=6.935A
6.2A FOR PCH
0.105A FOR VCCSSC
0.5A FOR VCCPLL
0.08A FOR VCCDMI

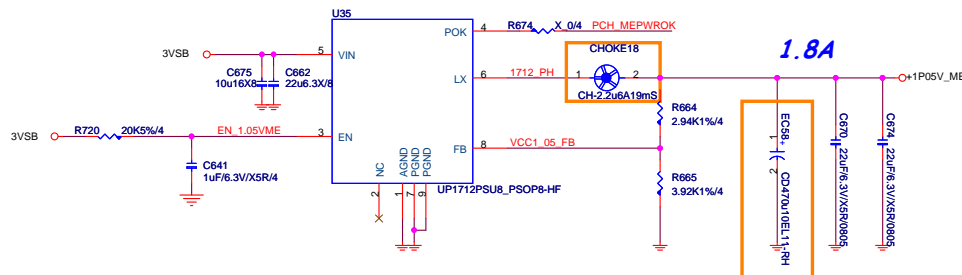


SLP_A

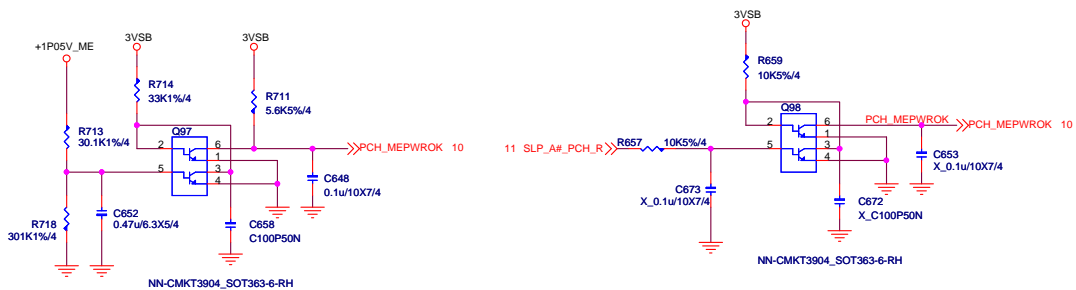


ME Power Control

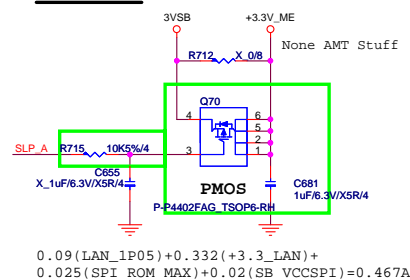
+1.05V_ME(VCCIO_ME)



PCH_MEPWROK



+3.3V_ME



MICRO-STAR INT'L CO.,LTD

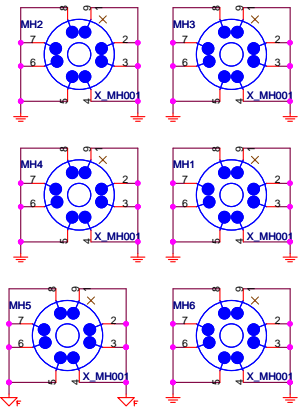
MS-7808

Size Custom	Document Description ME Power - UP1712	Rev 0A
Date: Friday, May 11, 2012	Sheet 35 of 41	

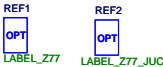
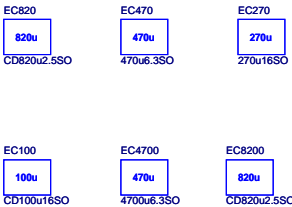
Mounting Holes



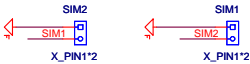
LA1
AMI_BIOS
LABEL
BIOS_LABEL



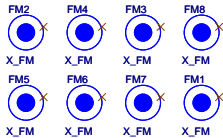
SOLID CAP



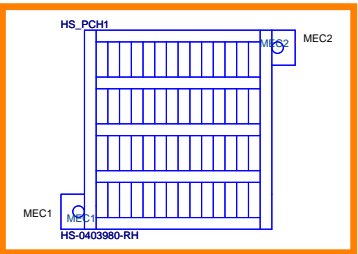
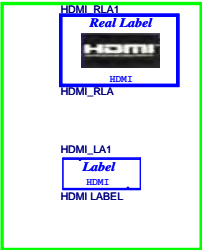
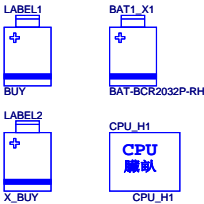
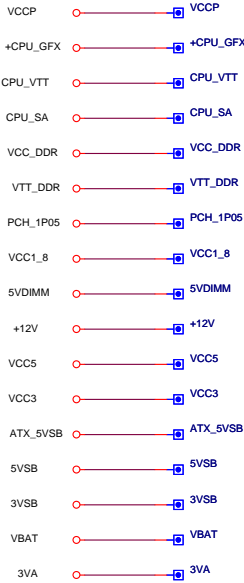
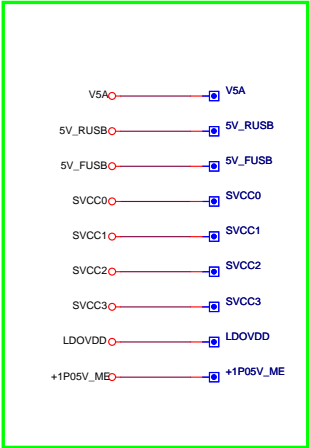
Simulation



Optical Fiducial Marks-120

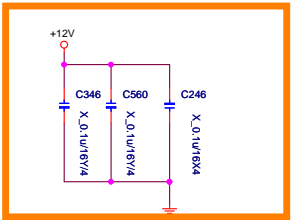
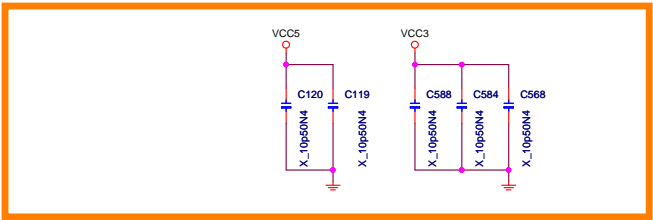


Voltage test point



EMI:cap. for signal return path

EMI



EMI